

Originally presented at IPC Advanced Packaging Symposium: "Building the IC-Substrate and Package Assembly Ecosystem" in Washington, DC, October 11-12, 2022.

Building the North American Advanced Packaging Ecosystem: Economic Challenges and Opportunities

E. Jan Vardaman, President and Founder

-  TRACK INNOVATION
-  IDENTIFY TRENDS
-  ANALYZE GROWTH
-  INFLUENCE DECISIONS

RELEVANT, ACCURATE, TIMELY

IPC Study Calls Out Need Critical Substrate Shortage Situation



AN ANALYSIS OF THE NORTH AMERICAN SEMICONDUCTOR AND ADVANCED PACKAGING ECOSYSTEM

Rebuilding U.S. Capabilities for the 21st Century



- **115 pg. report. Data rich analysis**
- **Influencing U.S. policy & investment**
- **‘Silicon to Systems’**
- **‘Manufacturing Matters’**
- **North America Key Findings:**
 - Ecosystem approach needed
 - No advanced IC-substrate capability or capacity
 - Lack of OSAT capacity (incl. bump)
 - ID critical systems/segments needed
 - No quick fix for today’s IC-substrate issues
 - Focus on next generation advanced packaging needs and know-how
 - Low labor cost (and incentives) drove assembly to Asia, need investment in smart manufacturing to bring it back!

North American semiconductor companies have migrated to the fabless model (Figure 1). The result is that the region is able to design next generation advanced packages but is heavily dependent upon Asian supply for chip manufacturing, IC-substrate production, and IC-packaging.

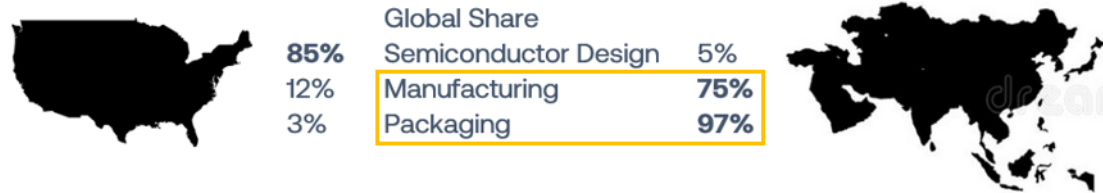


Figure 1: North American capability. Design focus, with outsourced manufacturing. Source: DoD Presentation

Key Messages

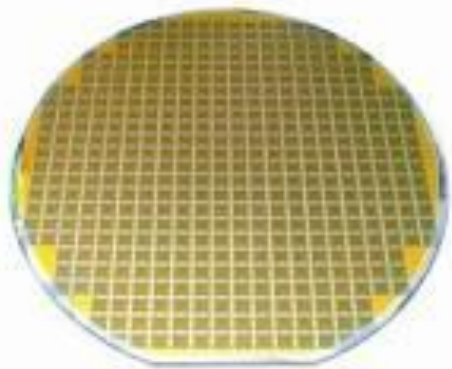
- Identification of **Critical Systems** and a **'Silicon to Systems'** approach are imperative for a sustainable ecosystem
- **If we don't take a broader ecosystem approach, we are lengthening the supply chain, not shortening it.**
U.S. built chips will be shipped to Asia for final component packaging (substrates, OSAT)
- Not being able to manufacture in North America **significantly slows down R&D cycle times**. Slower innovation.
- **To ensure resilient final systems production we cannot forget about high-mix, low volume North American-based PCB and ECAT needs, capability, and capacity**
- **Factory of the Future and new ways of working are needed to combat NA cost constraints.** Highly efficient, automated, data rich operations are needed to deliver high yields, high quality/reliability next gen electronic products

Matt Kelly, Chief Technologist IPC

Semiconductor Fabs: Necessary but NOT Sufficient Solution

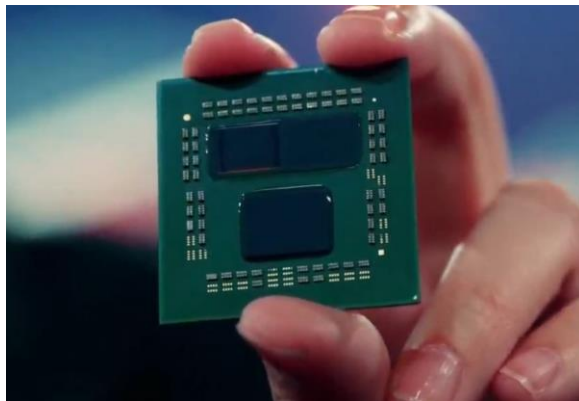
- **A package acts as the interface or intermediary between the chip and the board**
 - You can make all the silicon chips you want, but if you can't package them they don't do you much good!
 - If you don't invest in the packaging infrastructure in North America, what is the point of making the chips here if you just send them overseas for assembly?
 - You have not solved the problem, you lengthened the supply chain instead of shortening it

Silicon Wafer



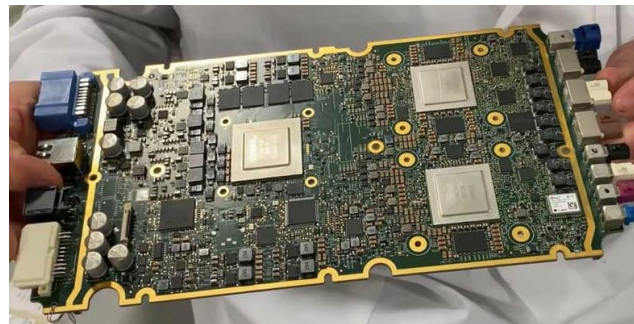
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Package with Build-up Substrate



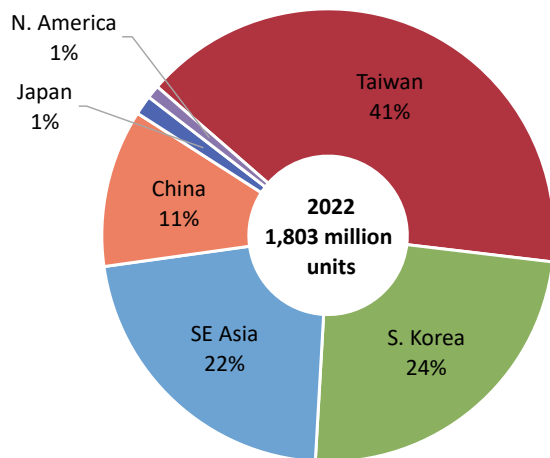
Source: AMD.

Board-Level Assembly (Tesla)



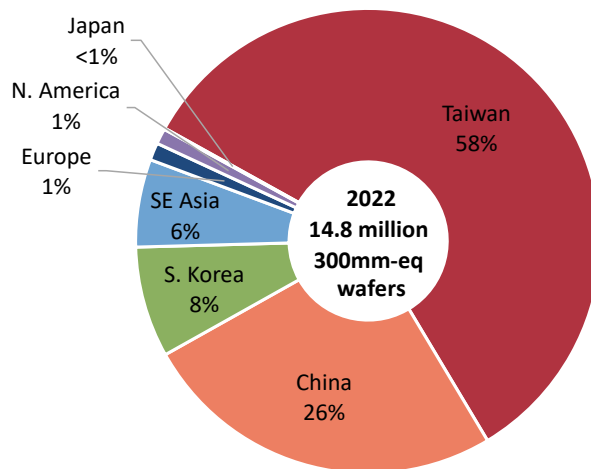
Problem: We Lack Build-up Substrate Capability, Advanced Packaging Assembly, and 300mm Bumping

FC-BGA Assembly by Region



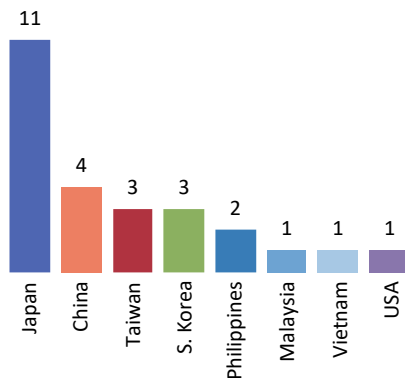
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Merchant Bump Capacity by Region



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Build-up Substrates Plants



Many Different Packaging Options: All Use Build-up Substrate

- **Silicon Interposers**

- Xilinx (many FPGA products) started in 2012, AMD shipped in 2015 (GPU + HBM), NVIDIA (GPU + HBM), Google, Baidu, Broadcom, many others in production!

- **Fan-Out on Substrate**

- Chip first (in production since 2016 at ASE) and chip last solutions (many designs)
- In production for network switch at TSMC with InFO-R (since 2018)
- Amkor Substrate-SWIFT®, SPIL Fan-Out Embedded Bridge, TFME

- **Embedded bridge Intel, IBM, SPIL, TSMC, and others**

- Intel's EMIB silicon bridge in an laminate substrate, embedded by substrate supplier (Intel Stratix 10 for AI accelerator)
- Amkor, ASE, IBM, JCET, SPIL, TSMC offerings

- **RDL Interposers Samsung R-Cube™ and others**

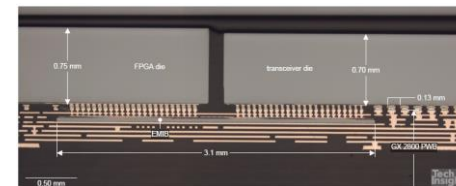
- Extend to finer feature (2μm L/S) switch to fab-like process

- **3D stacking**

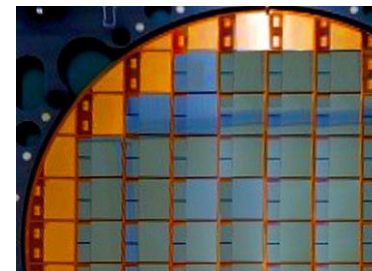
- AMD's 3D V-Cache™, Intel's Foveros, Samsung's X-Cube



Source: NVIDIA.



Source: Intel by TechInsights.



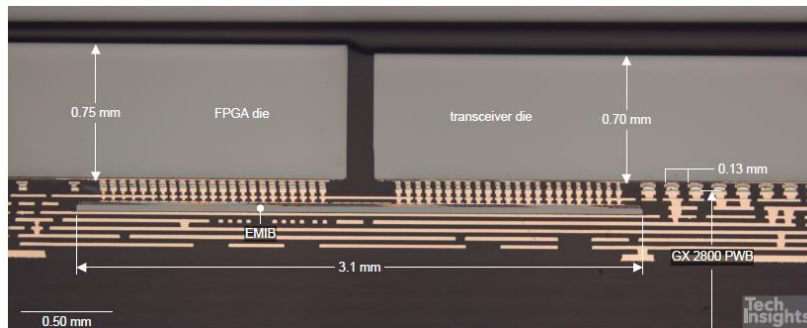
Source: ASE.

Intel's Embedded Multi-die Interconnect Bridge (EMIB)

EMIB size compared to grain of Basmati rice



Source: Intel.



Source: TechInsights.

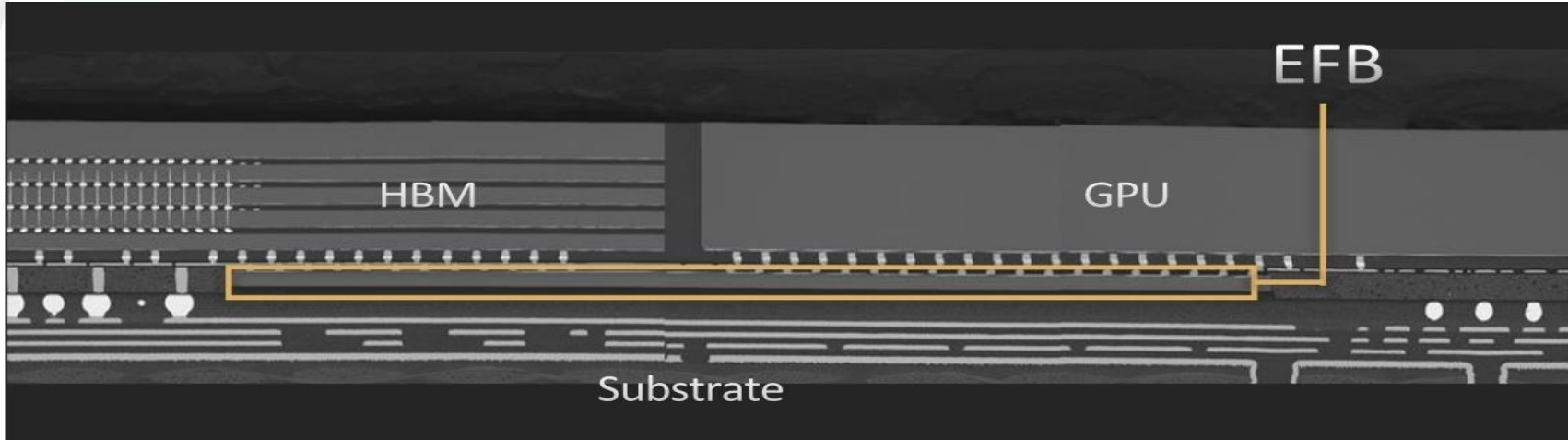
Sapphire Rapids first Intel server CPU with chiplets



Source: Intel.

- **A small silicon bridge chip is embedded into the package (no TSVs) to provide in-package, high-density connection**
 - Bridge die, designed and fabricated by Intel, embedded in the laminate substrate
 - Build-up substrate is 9/12μm L/S, up to 11 build-up layers on each side
- **Intel's Sapphire Rapids will be Intel's first CPU server for data centers using chiplets**
 - All 4 chiplets will access shared cache and are connected using the modular die fabric (MDF)

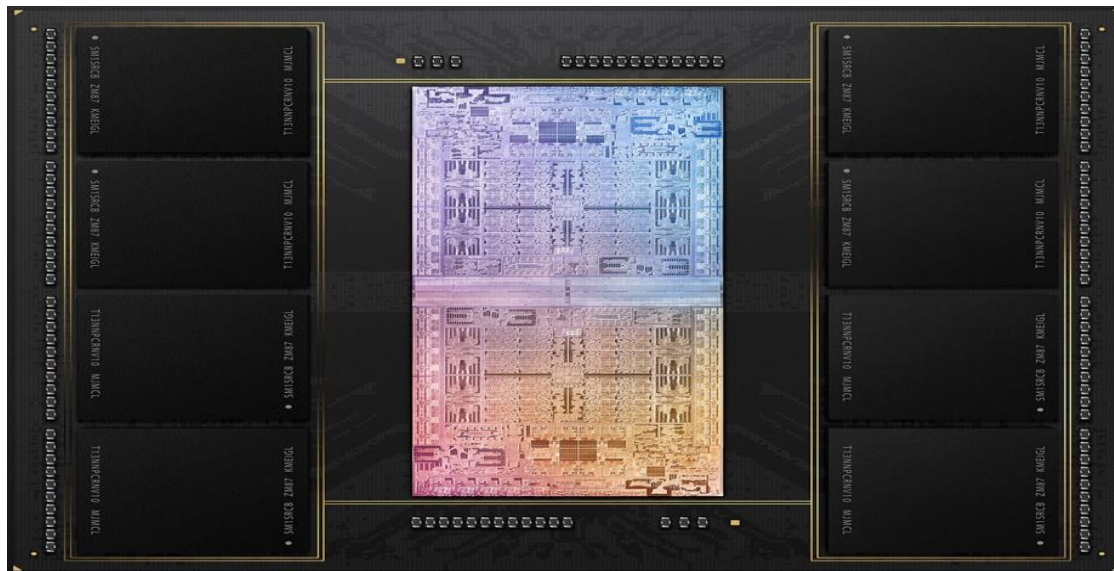
AMD's Elevated Fanout Bridge Technology



Source: AMD.

- **AMD's elevated fanout bridge (EFB) technology in production for machine learning applications such as core modules for the Frontier supercomputer**
- **Structure uses RDLs with EFB in the shadow of the Cu pillars**
- **Package substrate is 5-2-5 build-up with 14 μ m L/S**
 - Higher yield with less complex substrate
 - Less complex substrate possible because EFB used for communication between HBM and GPU

M1 Ultra for Apple Mac Studio Desktop



Source: Apple.

- **Packaged in TSMC's InFO_LSI**
 - Two M1 Max chips connected with silicon bridge
- **65mm x 65mm build-up substrate to form package**
 - Substrate uses 9/12 μ m L/S

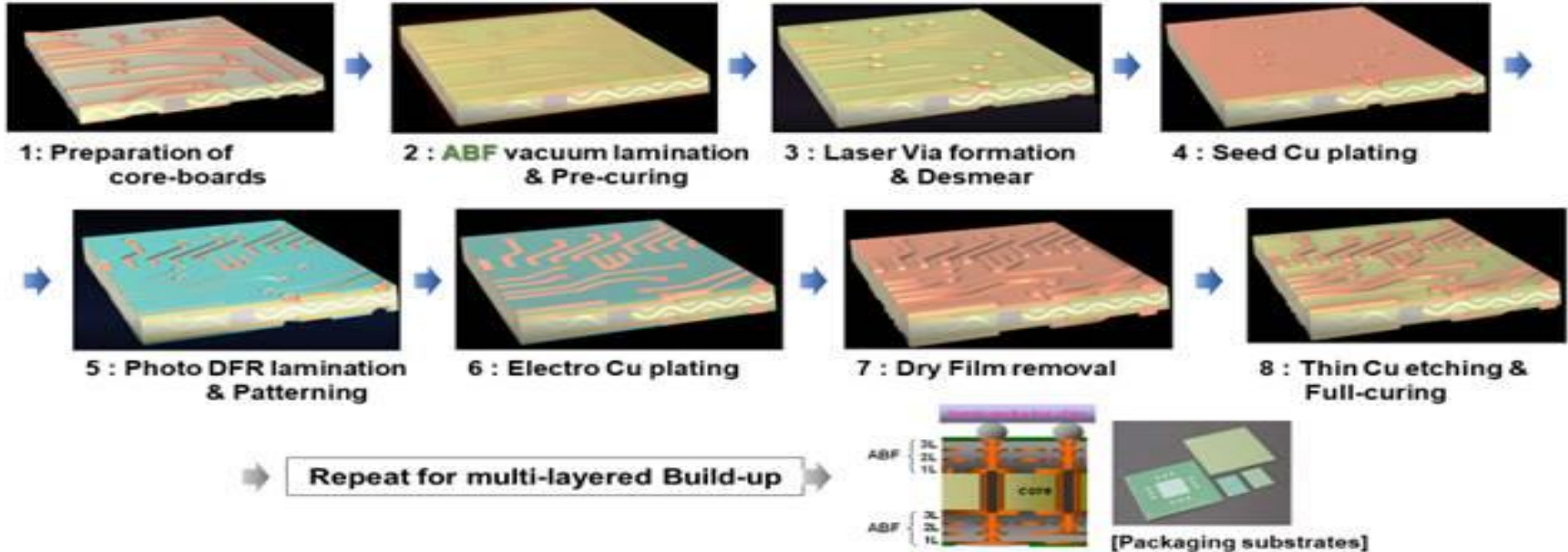
What is a Build-up Substrate?

Eat Well, Live Well.



AJINOMOTO

Outline of Manufacturing Substrates using ABF



8/02/2021

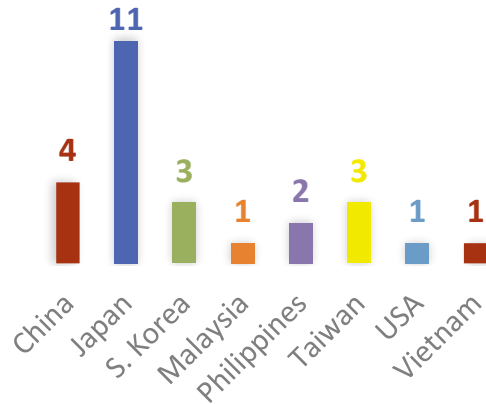
Proprietary and Confidential of AJICO

- Build-up substrate is fabricated by laminating layers of build-up film onto a core substrate fabricated from laminate material and copper

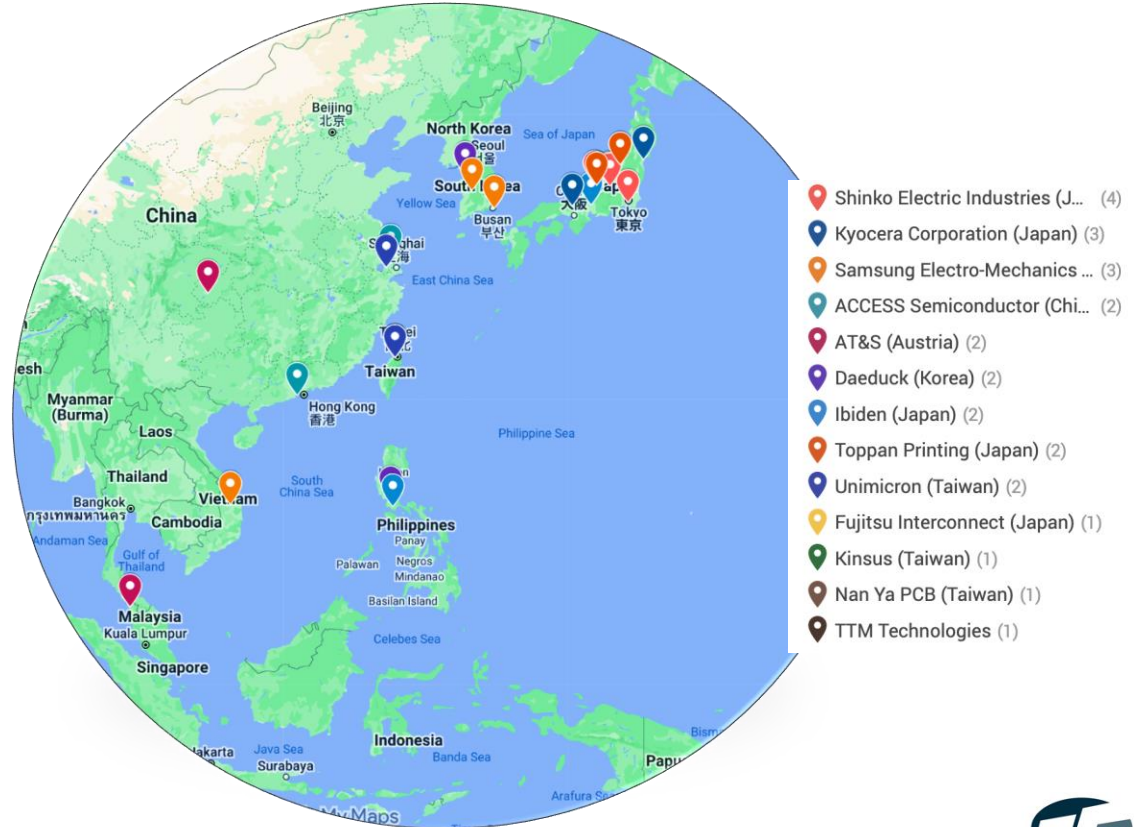
- Each layer requires a pass through the production line

FC-BGA Build Up Substrate Suppliers Globally

- 13 Companies in FC-BGA build-up
- 26 MFG sites globally
- Japan with 11 MFG sites
- Most are in Asia-Pac
- TTM is in the USA



Source: TechSearch International, Inc., October 2022.



Major Build-up Substrate Supplier Capability

Company	Min. Bump Pitch (μm)	Via/Pad (μm)	Min. Line Width/Space on Build-up (μm)	Core Via/Pad (μm)	Max. Build-up Layers (each side)	Max. Core Layers
ACCESS	150	60/95	15/15	-	3	2
AT&S	110	40/-	8/8	-	5	2
Daeduck	110	50/75	8/10	100/200	6	2
Fujitsu Interconnect	112	50/70	12/12	100/200	14	14
Ibiden	90	40/65	7/8	80/180	11	12
Kinsus	130	60/85	9/12	125/225	8	4
Nan Ya PCB	110	55/80	10/10	100/200	10	4
Samsung Electro-Mechanics (SEMCO)	100	49/77	9/12	120/270	7	4
Shinko Electric	90	45/70	8/8	80/180	9	2
Shinko Electric (prototype)	45	38/62	3/3	70/175	10	2
Toppan Printing	130	60/85	9/12	105/200	9	4
Unimicron	90	35/66	8/8	100/190	11	6

U.S. Has Not Made Major Investments in Build-up Substrates

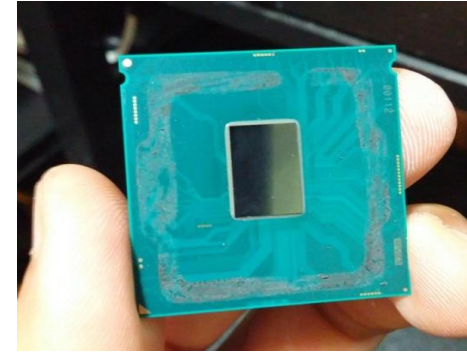
- **Many years ago, U.S. PCB makers decided not to invest in IC package substrate production**
 - Endicott Interconnect had some capability in U.S. but unique material set (sold to TTM)
- **Almost no capability in the U.S. to produce the most advanced IC substrates using build-up film to support high-density**
 - Substrate supplies concentrated in Japan, Taiwan, S. Korea, and a few in China
 - Some capacity in Philippines and Vietnam, planned for Malaysia
 - A few small suppliers located in U.S. but not with capability to support existing high-performance computing customers such as (Intel, AMD, Cisco, Broadcom, etc.)
- **Advanced IC substrate requires state-of-the-art know-how, equipment, materials, and processes**
 - Most equipment and material suppliers located in Japan, rest of Asia, a little in Europe
- **OK to use global supply chain, but...**
- **Adding domestic semiconductor fab/foundries without a domestic IC-substrate supply and OSAT assembly will lengthen the supply chain, not shorten it**

2021 Substrate Capacity Constraint Was A Nightmare!

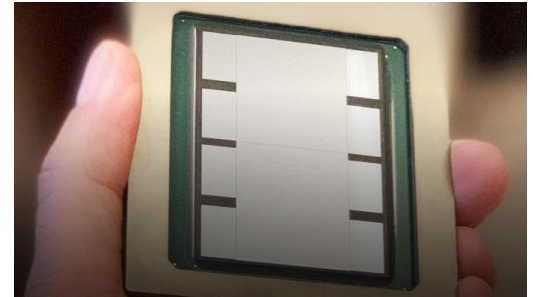
- **FC-BGA substrates were in short supply in 2020-21**
 - Capacity was tight by end of 2020, especially with Unimicron fire and accident at Kinsus
 - Shortages driven by body size increase, not unit volumes
 - Qualification process for new suppliers and materials is long and expensive
 - Some laminate substrate production equipment has long lead times of 1-2 years
- **Prices for IC package substrates increased and lead times stretched out**
- **Substrate suppliers have been reluctant to increase capacity for fear of over capacity**
 - New production line is expensive
 - Substrate makers had relatively low GM
 - Substrate suppliers were treated poorly by customers
 - We must stop treating advanced substrates as a commodity!

Laminate Substrate: Increased Demand for High-Performance

- **Datacenter and cloud computing use high-performance semiconductors and advanced packages**
 - Driving Flip Chip-Ball Grid Array (FC-BGA) substrate capacity expansion
- **Server CPU**
 - Increased layer counts (18-22 build-up layers)
 - Largest body sizes 72 mm x 75.4 mm, 56.5 mm x 77.5 mm
- **AI accelerator demand increasing**
 - Si interposer, Embedded Bridge in substrate
 - All use laminate substrates to form the package
 - Largest body size today is 77.5 mm x 77.5 mm
- **Networking switch products**
 - Increasing from 91 mm x 91 mm to ≥ 100 mm x 100 mm
 - More complex with higher layer counts

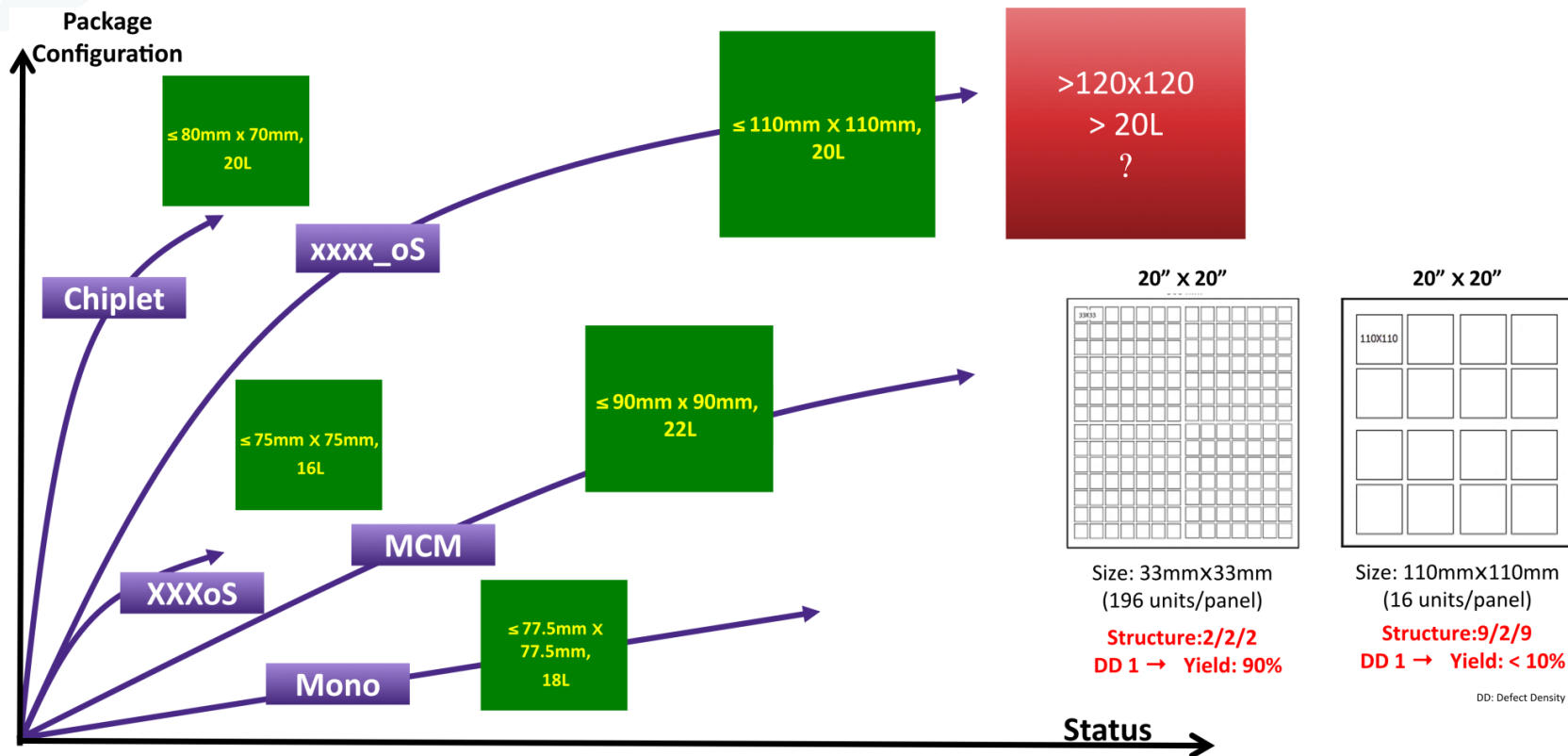


Source: Anandtech.com



Source: TSMC.

Large Substrate Body Size Requires More Capacity

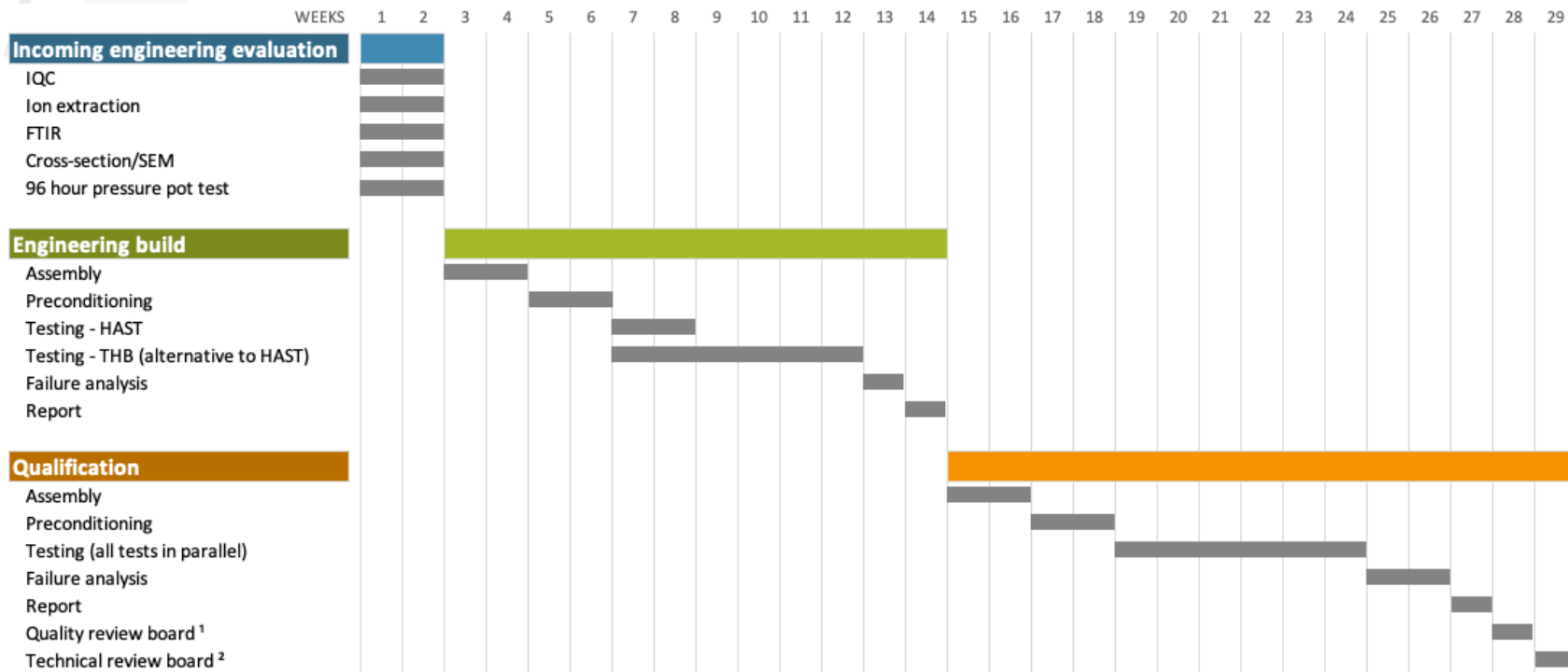


- Need more capacity to meet the high-performance, large body size requirements

Substrate Landscape – Low Margins Limited Investment

- **Level of investment required for next generation substrates is difficult for substrate manufacturers to meet with their low margins**
 - Gross margins for Foundry ~41% vs. 22% for substrate supplier group with representative company from each region (Japan, S. Korea, Taiwan)
 - Investment now because customers supporting
- **Build-up capacity expansion plans underway AT&S, Ibiden, Kinsus, Kyocera, Nan Ya PCB, SEMCO, Shinko Electric, Toppan, and Unimicron**
 - Ibiden tearing down the existing Gama plant and bring new capacity online in 2026
 - Domestic China suppliers such as Shennan Circuit (SCC) and PCB maker ZDT (Avery) also plan build-up substrate production
 - SEMCO will convert an RF module plant in Vietnam to FC-BGA, capacity will be online starting in mid-2023 with much of the capacity dedicated to a single customer
 - Shinko Electric announced a \$1.4 billion expansion plan that will add capacity as early as 2024, specifically targeted for a specific customer

Flip Chip BGA Substrate Qualification Gantt Chart

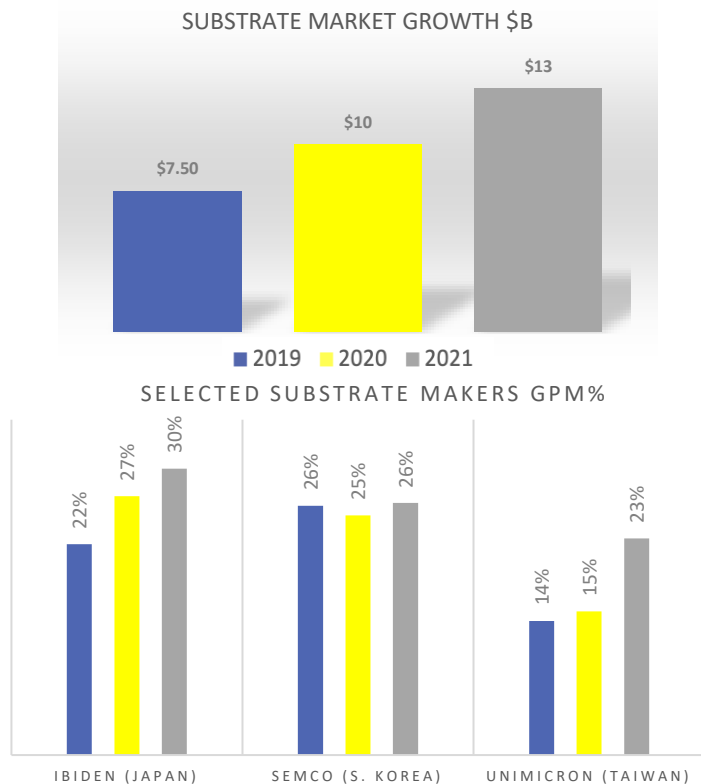


(1) engineering review of qualification results

(2) manufacturing capability demonstration

- On average, takes 25 weeks and \$250,000 to qualify a new substrate vendor under perfect conditions (Several companies indicate the average time is more than a year)

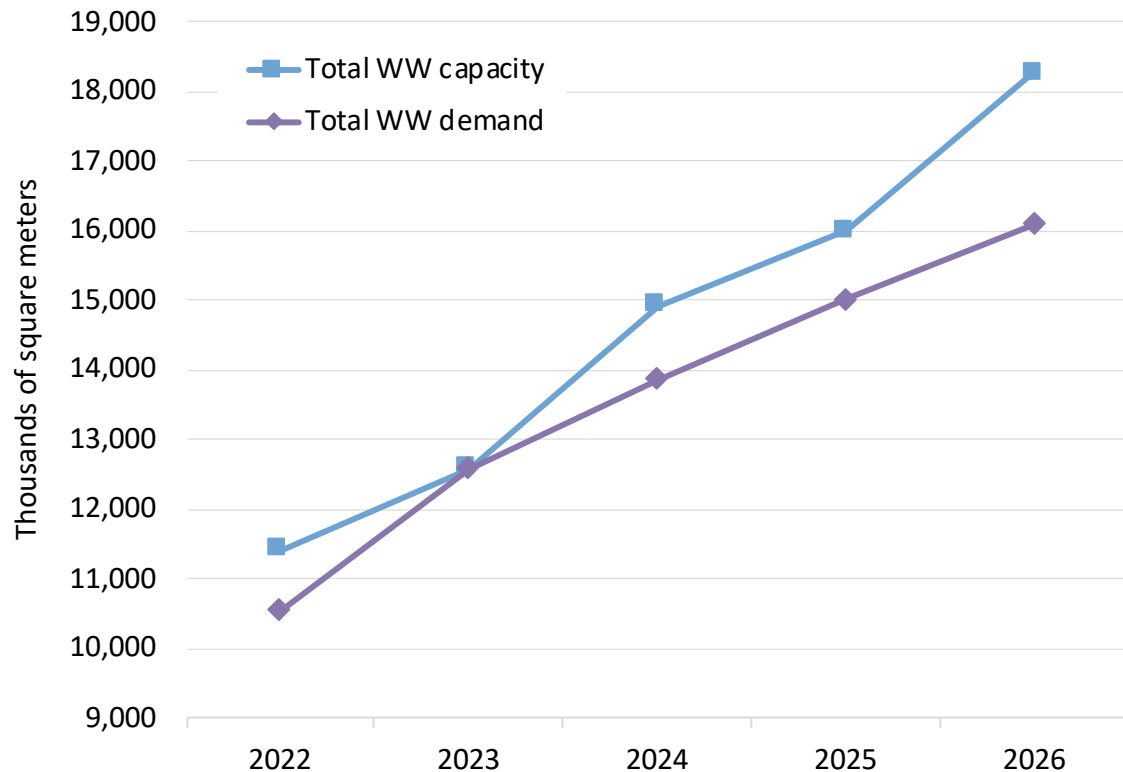
Good News! Substrate Industry Shows Signs of Improvement



Source: TechSearch International, Inc., adapted from company financial reports.

- **Revenue for IC package substrate companies increased by 73% 2019 vs 2021**
- **Improvements are attributed by:**
 - Currency fluctuations
 - Demand for the more complex, i.e. more expensive designs
 - Larger body substrates
 - Price increases
- **The substrate industry is becoming healthier, as reflected in the higher gross margins for most companies reported in 2021**

Shortage for FC Build-up Substrates Will End!



Falling demand eased the substrate shortage this year

- Substrate makers are not requesting “non-refundable deposits” with substrate order

An oversupply situation will occur in starting in 2024 assuming the substrate sizes do not exceed 100 mm x 100 mm for CPUs and 110 mm x 110 mm for network switch

- Larger substrate sizes or lower yields will erase the surplus

Industry will want to return to “business as usual” pushing down on price and become unwilling consider new players

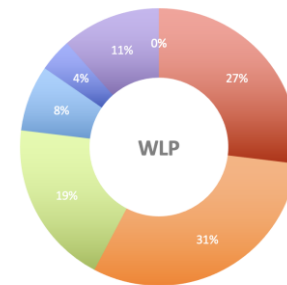
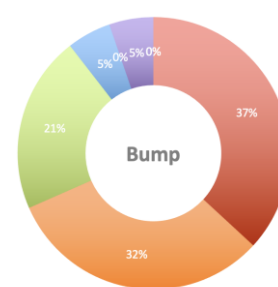
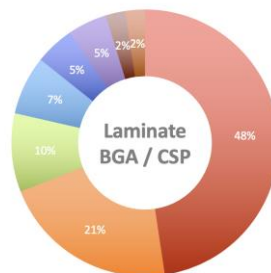
Outsourced Assembly and Test Services

World Wide Bump and Advanced Assembly Sites



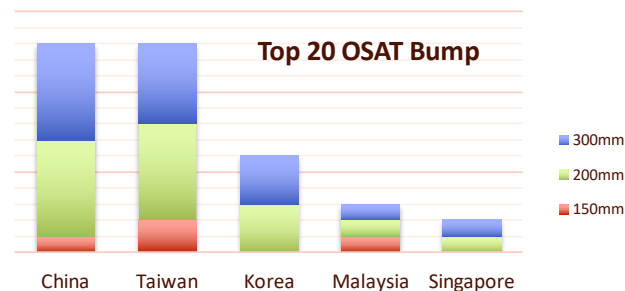
Source: TechSearch International, Worldwide OSAT Manufacturing Sites Database, updated October 2019

- **Top 20 OSAT comprise >90% of the total advanced packaging worldwide**
- **Top 20 Global Advanced Packaging and Bump Capability resides in Asia Pacific Region**



China Taiwan Korea Singapore Japan Malaysia Indonesia Philippines

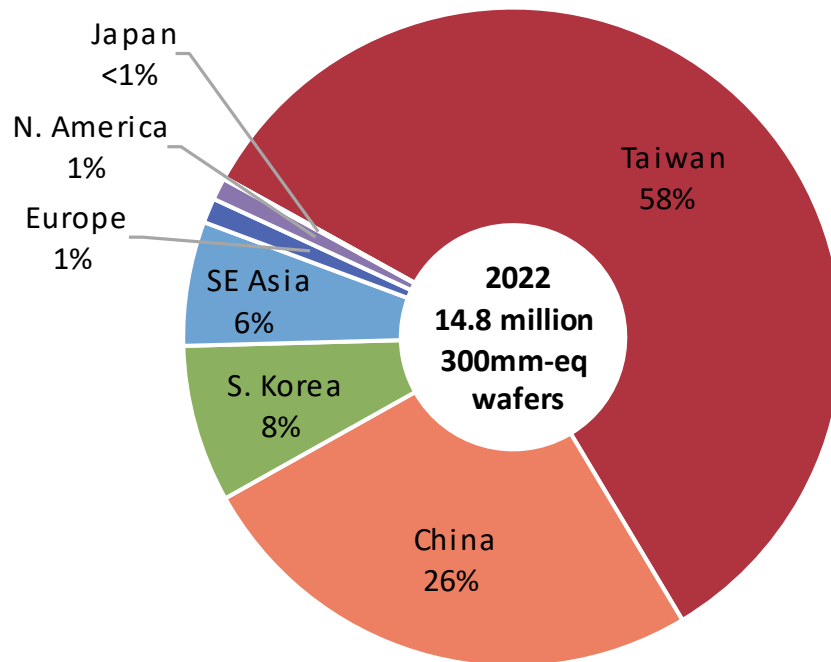
Source: TechSearch International, Worldwide OSAT Manufacturing Sites Database, updated October 2019



Many Small OSATs Located in U.S.

- **Small to medium assembly operations with good capabilities, but not high volumes (100,000 to few million units per year vs. billions of units/year)**
 - Many of these companies offer wire bond on leadframes or laminate substrates
 - Assembly for advanced packaging includes bump, assembly, and test and this is lacking in U.S.
 - No qualified high-volume 300mm bumping with the exception of internal capacity at semiconductor companies
- **Some semiconductor companies with internal assembly, but few sites in North America**
 - Exceptions: Skyworks in Mexicali, Mexico for components for smartphones, Intel will install assembly in New Mexico, TI has internal capability, Qorvo has internal capability, Northrup Grumman for military

We Have No Merchant 300mm Bumping Capability in U.S.



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- While there is sufficient captive capacity for bumping, merchant bump capacity is needed in North America

Most Assembly in North American Is Not Advanced Packaging

- **IBM Assembly and Test located in Bromont, Canada**
 - Advanced packaging capability including flip chip and photonics assembly
 - Successful operation
- **Some smaller companies with good capabilities**
 - Mostly wire bond
 - Many providing assembly for defense sector
 - A few with flip chip assembly, but limited capability
 - Increased interest in offering flip chip assembly, but need customers!



60mm x 37.5mm package with 400 μ m laminate core

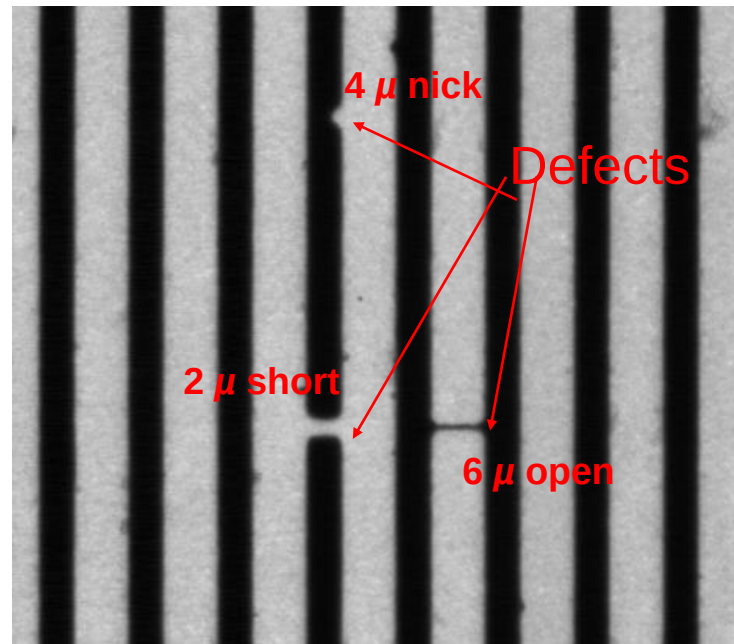
23 different part numbers (195 on top side, 247 on bottom)

High component density with limited spacing

What Can We Do?

Yield Improvement for Substrate Production!

- **Focusing on manufacturing technologies is key**
- **Factory of the future needed**
 - Takes place under cleanroom conditions
 - Automated process reduces labor content and cost, improves yield
- **Backend needs to make use of metrology as has been done in fab**
- **More parts per panel = greater available capacity**
- **Improvement in substrate design to allow for higher yields?**
 - Layer counts?
 - Fine traces?



Source: Beltronics.

Measurement Density for Inline Metrology System



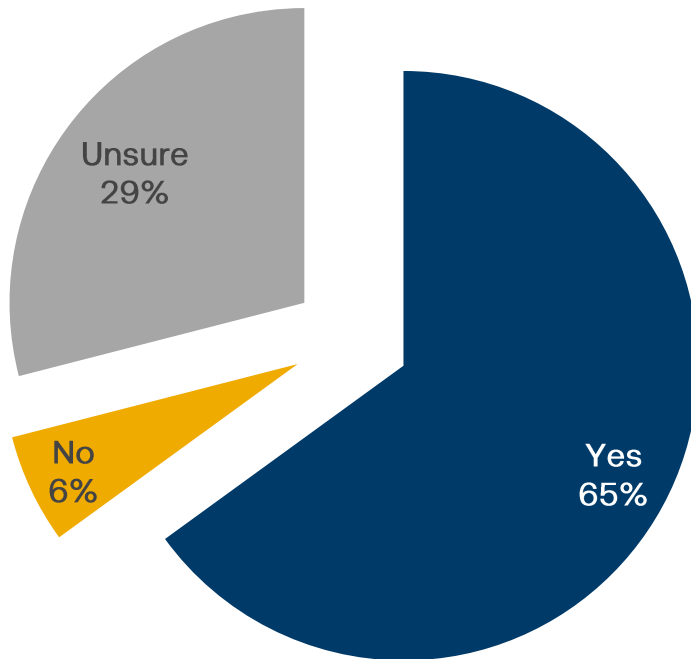
Source: Beltronics.

- **An inline metrology method for substrate production quality control enables 10 billion line/space measurements to be performed over a 500mm x 510mm panel in 5 minutes with 0.15 μ m accuracy**
 - Defects are detected by comparing scanned images to CAD files
 - Data analytics (Data is stored and collected for analyzing and modeling the substrate manufacturing process)
 - Compensates for reference misalignment during inspection to eliminate false calls
 - Fluorescent imaging used to eliminate brightness intensity variations due to metal grain and texture and to detect organic contaminant
 - New search-locate-measure image analysis method used to solve fine feature alignment issues

U.S. Needs Substrate Production: Customers Must Commit

- **Need high density substrates (some level of build-up substrate production)**
 - U.S. Defense (today may not need high density, but need domestic source of substrates)
 - Medical
 - High Performance Computing
 - Start-ups (long lead times means you can't test out new designs)
- **Companies say will purchase substrates made domestically if:**
 - Made by existing qualified substrate supplier
 - Relatively competitive price (defense and quick-turn pays more)
 - U.S.-based supplier should concentrate on advanced substrates to meet future needs
 - Why try to compete with well established Asian suppliers?
- **Future advanced substrate production could be an export product**
 - “Specialty Steel”
 - Most advanced substrates made in Japan, but customers are not in Japan!

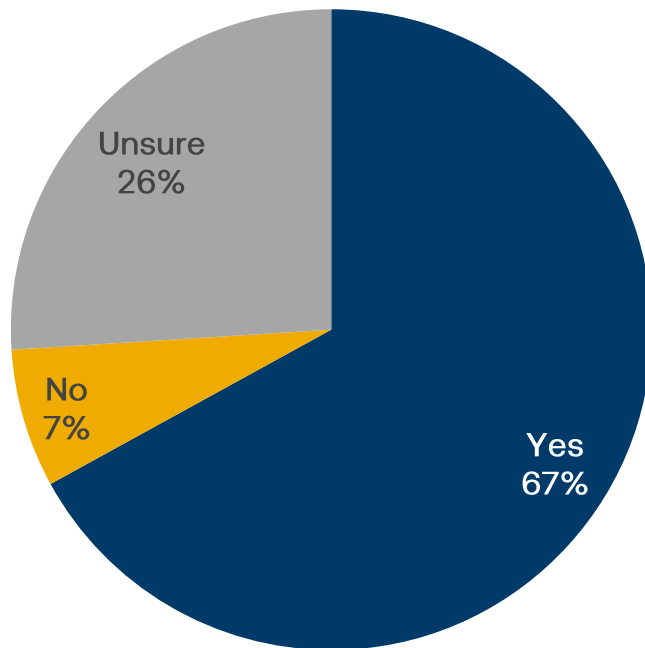
Will Companies Purchase U.S. Made Substrates?



Source: IPC.

- **What is your company's likelihood to purchase: Cost-competitive advanced IC package substrate available from U.S. sources?**

Will Companies Use U.S. IC Package Assembly?



Source: IPC.

- **What is your company's likelihood to use: Cost-competitive advanced IC package assembly available in the U.S.?**

Invest in Factory of the Future and More!

- **Increased use of AI and machine learning**
- **Invest in assembly for the future advanced packages**
 - Emerging areas such as co-packaged optics have challenges that can be met with focused effort
- **Understanding of why manufacturing moved away from U.S.**
 - Tax reasons
 - Cheap labor (automation reduces labor cost)
- **Sustainability is important!**
- **Dial 911 for manufacturing help**
 - Tap into the retired talent pool of people that have experience in manufacturing
 - Guest worker program to provide engineering and manufacturing talent

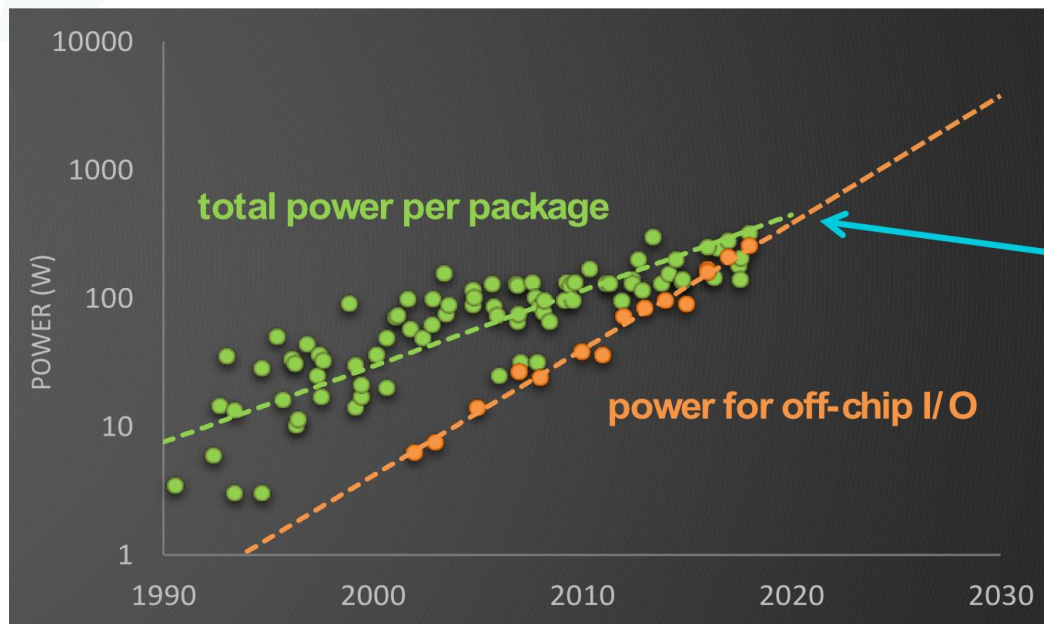


Source: Siemens.

Use of AI at the Edge in Smart Factory: Micron Example

- **AI to improve factory efficiency**
 - Need data analysis locally, at the factory
- **Deploy IoT platform for early detection with IoT sensors (image, acoustic, video)**
 - Infrequent events, detect low-frequency, high impact events
 - Automate root cause analysis and prescribe action
 - Example: Detect dispense of nozzle tip and nearby area, time period of dispense (if irregular, stop tool)
 - Install on tools, such as photo tools
 - “image analytics” detect deviation from standard to decrease variability
- **Large amount of data, visually examine**
 - 470,000 sensors
 - 13 terabytes of data
 - 15.6 million wafer images weekly
- **Automatically provide diagnostics**

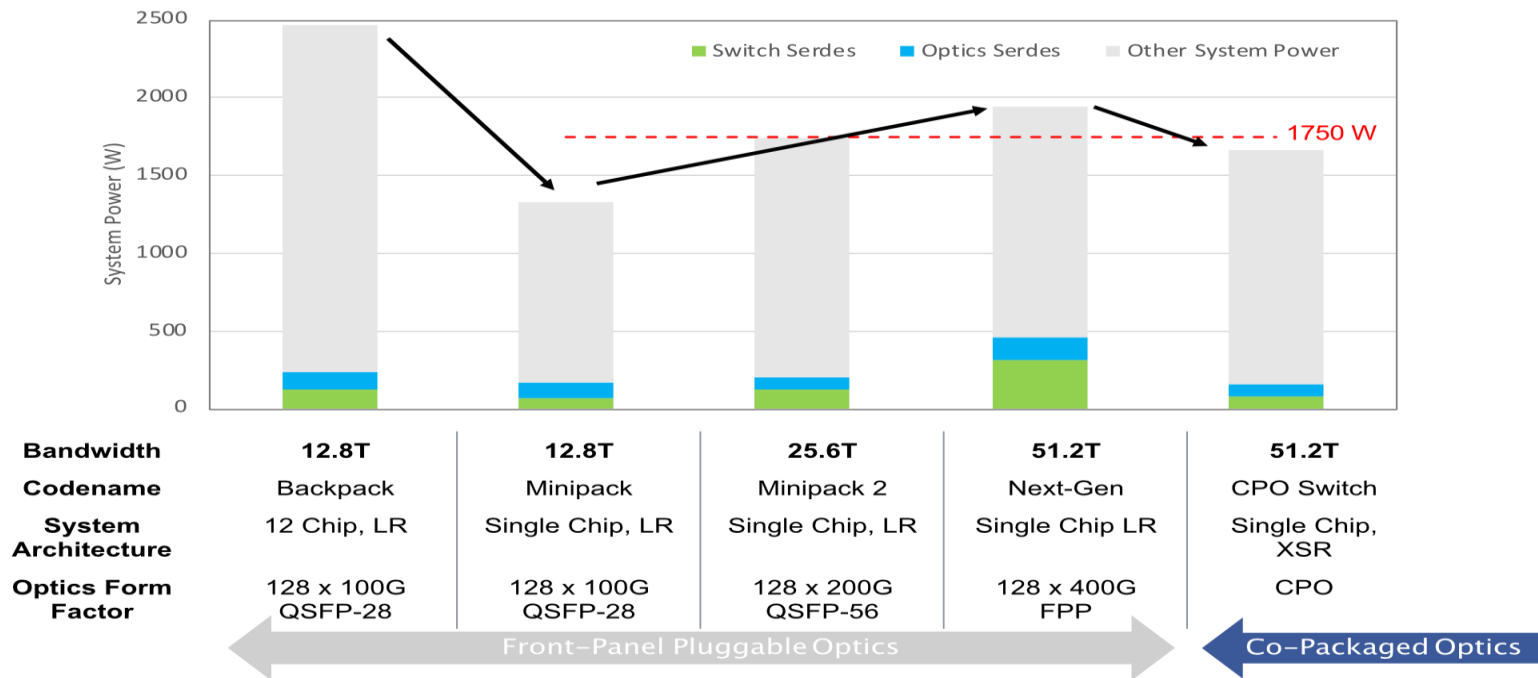
Most Challenging Problems in HPC: I/O Density and Power



[G. Keeler, DARPA ERI 2019]

- As bandwidth increases, energy efficiency per bit decreases, especially for network switch
- Half a chip's power is spent on data transfer (scaling transistors does not solve)
- Power budget is being consumed by electric SERDES interconnect
- Co-packaged optics proposed as a solution

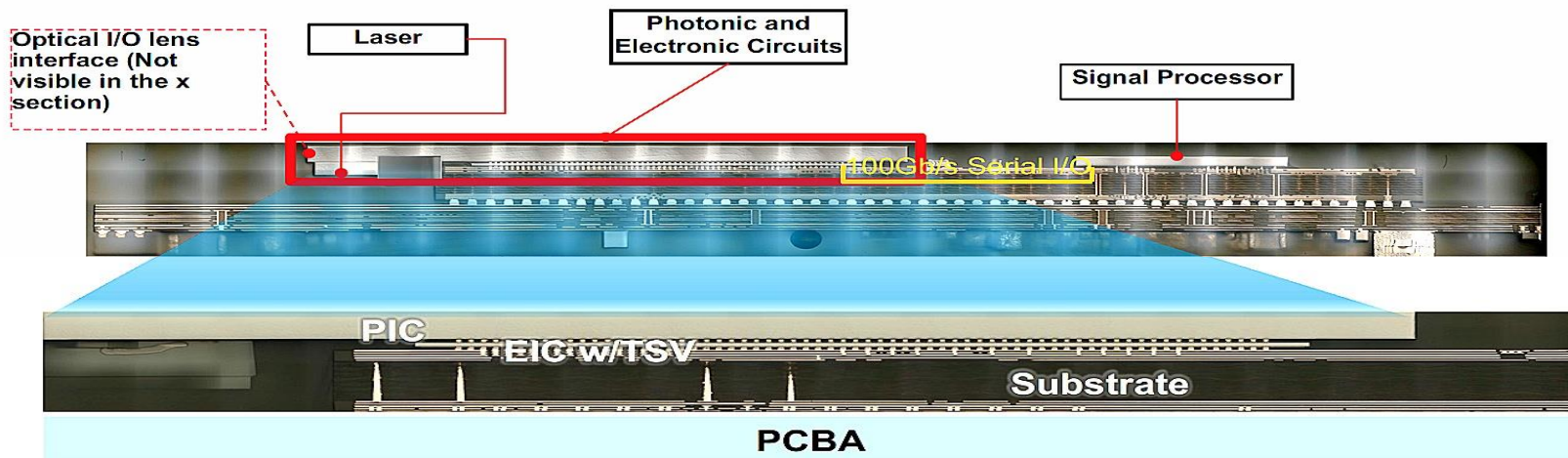
Drivers for Co-Packaged Optics at 51.2T



Source: IEEE 802.3 Beyond 400G Study Group.

- Advantages of CPO include improved energy efficiency and bandwidth density, reduced latency, and power efficiency
- Adoption of CPO needed for bandwidth at 51.2 Tb/sec and beyond

Challenges for Co-Packaged Optics



Source: A. Bjorlin, "Breaking the Bandwidth Barrier: Si Photonics Optical I/O," SEMI Americas Virtual Forum, 2021.

- **Fiber attach is greatest challenge**
- **Integrating lasers in the package or on the chip?**
 - Temperature can degrade laser, how to replace?
- **Shift from pluggable to BGA mounted on board or socketed solution?**
 - Need to be replaceable for upgrades and field repair, standards to lower the cost and manufacturing cycle time

Continued Investment is Required!

- **Top 4 OSATs continue CAPEX spending on test and assembly equipment, mostly for advanced packaging**
 - Advanced packaging revenue for top 4 OSATs in 2021 was \$25,396 million
 - Represents ~14.8% of revenue
- **TSMC spending on advanced packaging increases each year**
 - TSMC advanced packaging revenue in 2021 was \$4.1 billion

Top 4 OSAT CAPEX Trends (\$ in millions)

Company	2017	2018	2019	2020	2021	2022
ASEH	\$1,028	\$1,082	\$1,487	\$1,525	\$1,807	\$1,806
Amkor	\$551	\$547	\$472	\$553	\$780	\$850
JCET Group	\$628	\$648	\$407	\$487	\$625	~\$890
PTI	\$590	\$587	\$283	\$606	\$547	\$700
Total	\$2,797	\$2,864	\$2,649	\$3,171	\$3,759	\$4,246

Source: TechSearch International, Inc.

TSMC Revenue and CAPEX

	2019	2020	2021	2022
Net Revenue	\$34.63 billion	\$45.52 billion	\$56.82 billion	~Growth % in mid to high 20s
Total CAPEX	\$14.9 billion	\$17.2 billion	\$30 billion	\$40-44 billion
Advanced Packaging CAPEX	\$500-700 million	~\$1.6 billion (includes mask making)	~\$3 billion (includes mask making)	~\$4.0-4.4 billion (includes mask making)

Source: TechSearch International, Inc., adapted from TSMC.



“We choose to go to the Moon in this decade and do the other things, not because they are easy, but because they are hard, because that goal will serve to organize and measure the best of our energies and skills, because that challenge is one that we are willing to accept, one we are unwilling to postpone, and one which we intend to win, and the others, too.”

John F. Kennedy delivered his speech imploring America to reach for the lunar surface on Sept. 12, 1962.

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Thank you!

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