

Improvement of via connection reliability
by thinning electroless copper plating

OPC FLET PROCESS

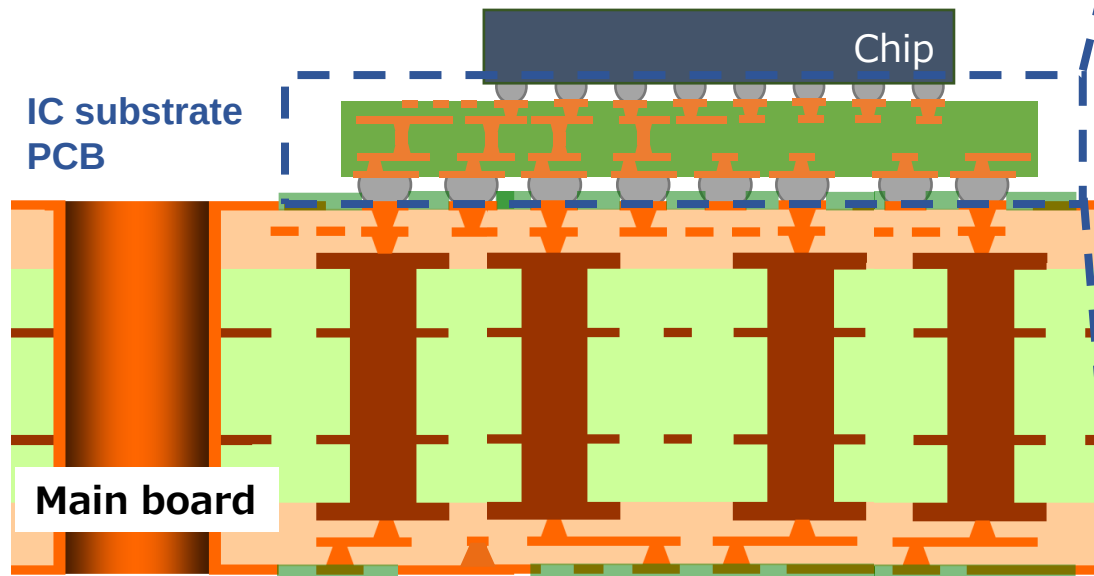
Okuno Chemical Industries Co., Ltd. (Osaka, Japan)

Naoki Okuno, Hidekazu Homma

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Trends in the latest IC substrate PCBs

Advanced performance in electronics



Size: μm	2023	2025	2030
Line/Space	5/5	2/2	1/1
Via diameter	30	10	5

Via : Diameter downsizing

Now

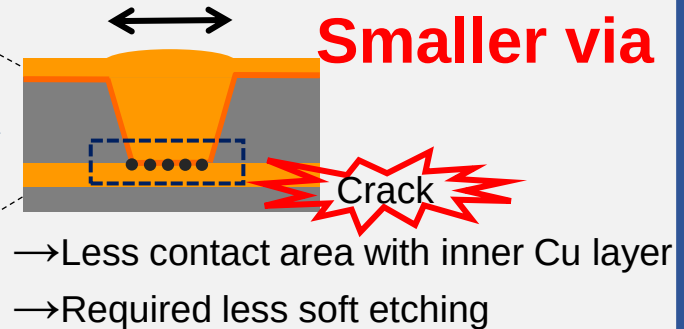
Diameter : 40-60 μm



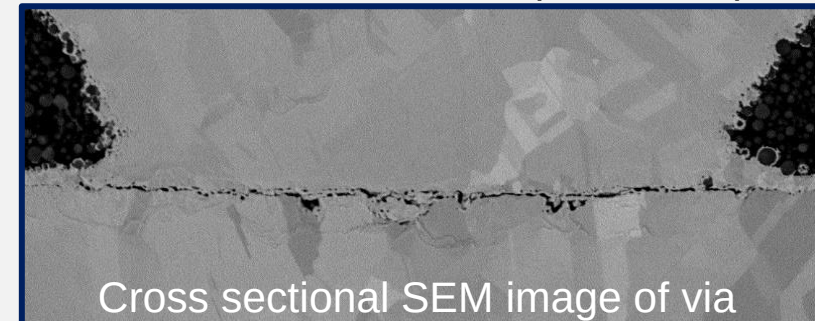
Cross section of Via

Future

- ① Diameter : Under 10 μm
- ② Inner Cu layer under 2 μm



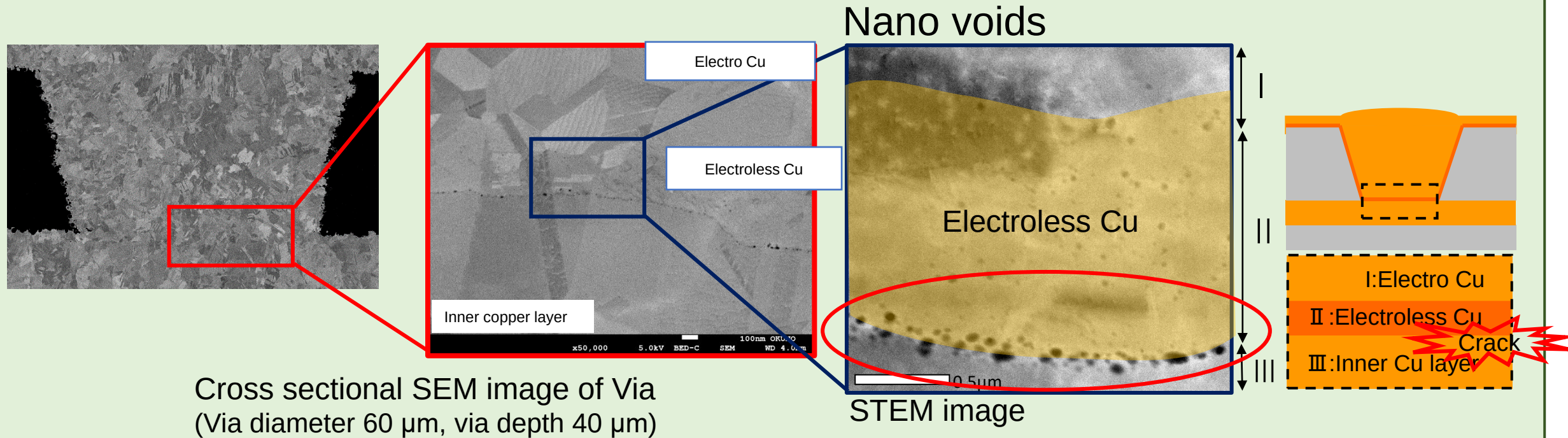
Via crack Via diameter 15 μm , via depth 15 μm



Cross sectional SEM image of via

Via crack / Issues with conventional electroless Cu plating process

Cross sectional observation of via after Cu electroplating in conventional process

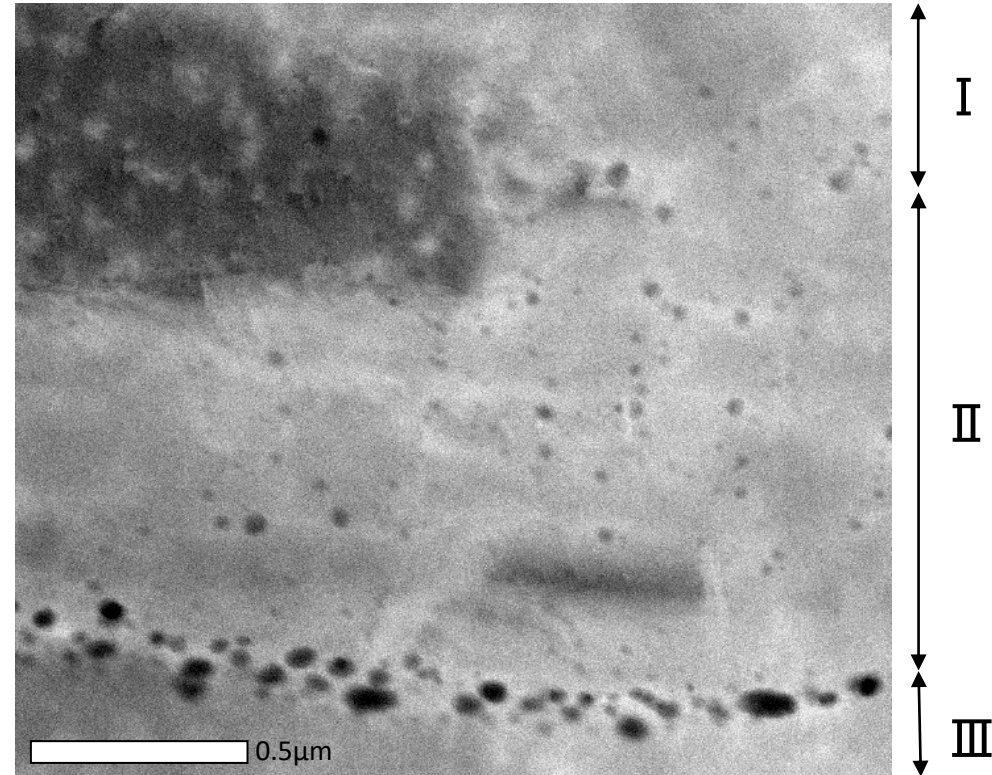
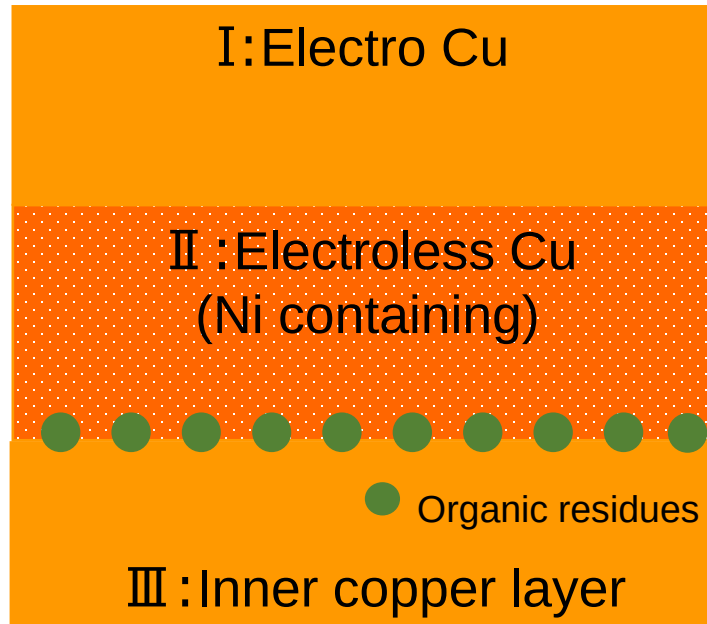


• TEM observation: Flexible 3D system Integration Laboratory at Osaka University

Via cracks are caused by nanovoids generated at the interface of the electroless Cu plating.

Nano voids

Conventional process



STEM image of via

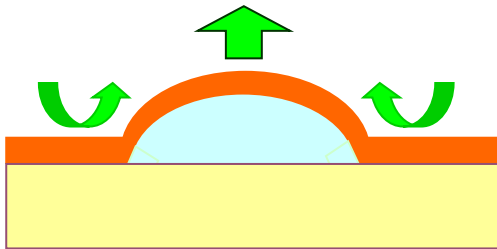
- Organic components: Many
- Nickel: Contained in film
- Hydrogen gas amount in electroless copper plating: Much

Conventional electroless Cu plating bath

Conventional bath Film Stress adjustment method

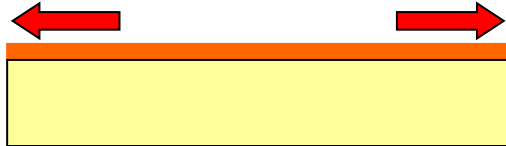
Compressive stress

The film to expand and spread, which leads to blister.



Tensile stress

The tensile stress acts as a pull on the outside.



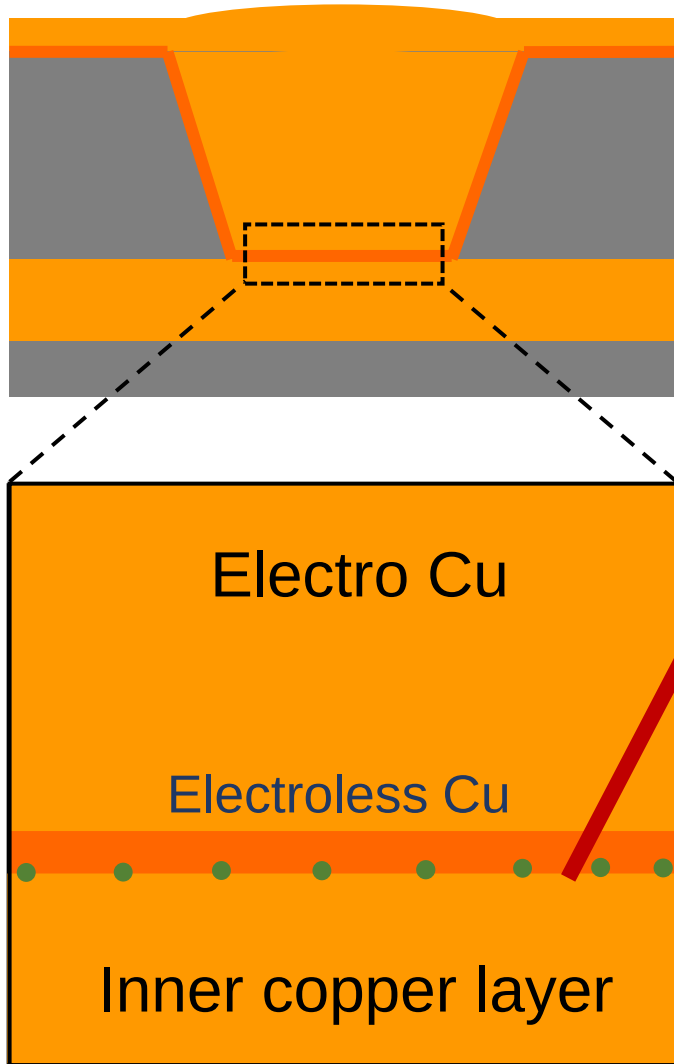
Nickel is co-deposited on the electroless Cu plating film to adjust to weak tensile stress.

Effect of nickel

	Conventional bath (Ni containing)	Ni free bath
Ni in electroless Cu (% by weight)	1.5	0
Film stress (1.0μm)	110MPa (Tensile)	-140MPa (Compressive)
Deposition on build-up film		
	No blister	With blister

Weak tensile stress solves blisters.

OPC FLET PROCESS



① Reduce organic components remaining on inner copper layers

② Ni free : Lowering deposition speed

Achieve high via connection reliability
by preventing nano voids

OPC FLET PROCESS

● Organic components from the pre-treatment of electroless copper plating

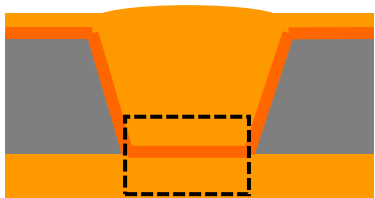
OPC FLET PROCESS

(Electroless copper plating process)

Step	Solution	Bath temp.	Treatment time	
Conditioning	OPC FLET CLEANER	50°C	5 min	①Reduce organic components residues Non-cationic component Weak anionic component
Soft etching	OPC FLET SOFT ETCH (Copper etching amount: < 0.05 μm)	25°C	1 min	
Desmutting	5% sulfuric acid	25°C	2 min	
Pre-dipping	OPC FLET PREDIP	25°C	2 min	②Nickel free film
Catalyzing	OPC FLET CATALYST	40°C	5 min	
Activating	OPC FLET REDUCER	25°C	5 min	Lower plating speed
Electroless Cu plating	OPC FLET COPPER (Cu 2.7g/L, pH 12.5, HCHO 5.0g/L)	27°C	10 min	

* Excluding after pre-dipping, water rinse is conducted after each step.

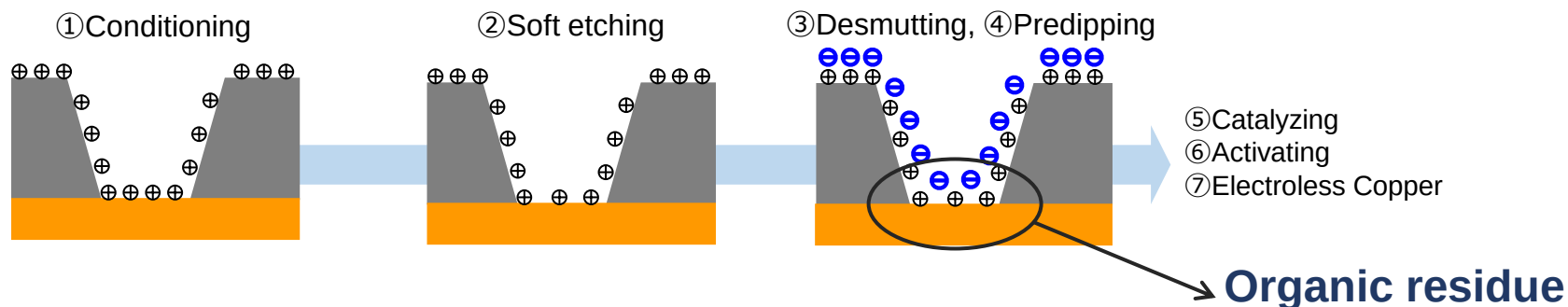
Organic residue on inner copper layer



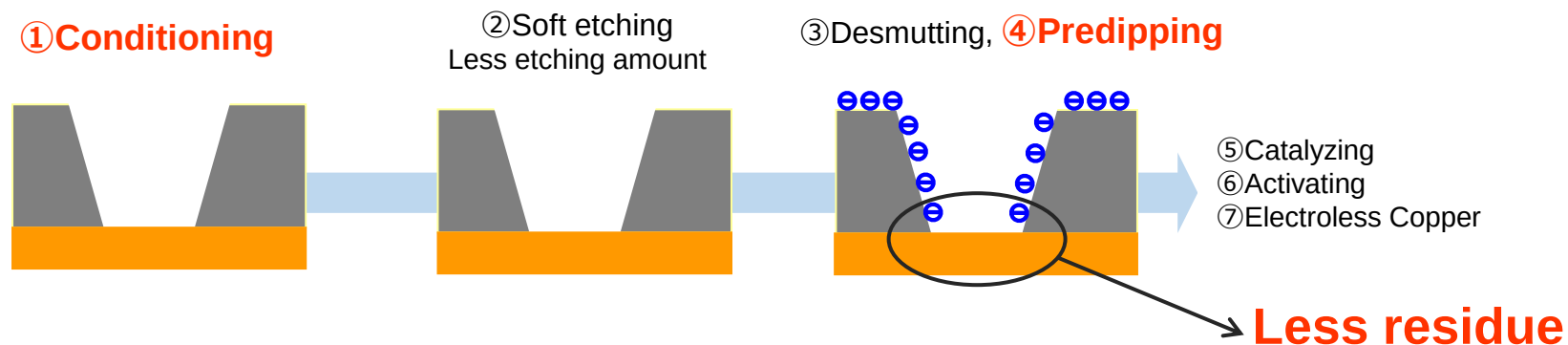
Organic residue on inner copper layer

Less organic residue derive from conditioner before electroless copper plating

Conventional process



OPC FLET PROCESS



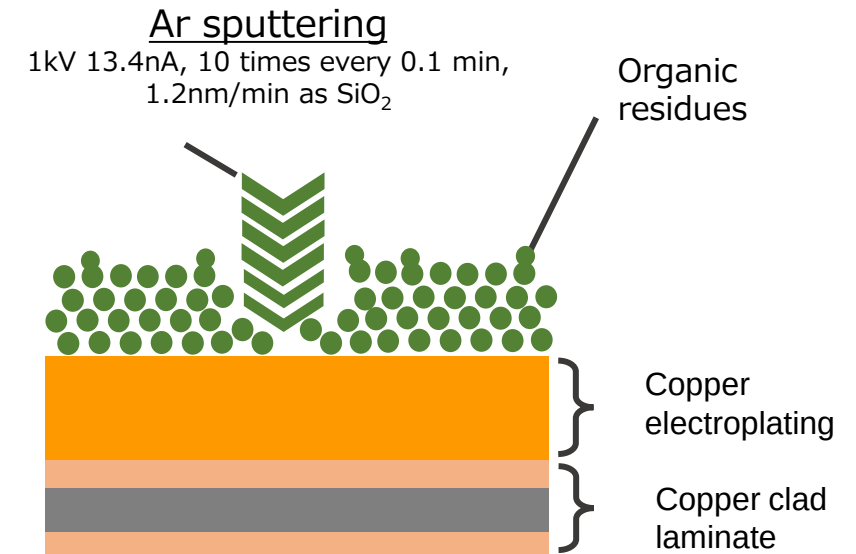
Organic residue comparison on inner copper layer

After activation

OPC FLET PROCESS

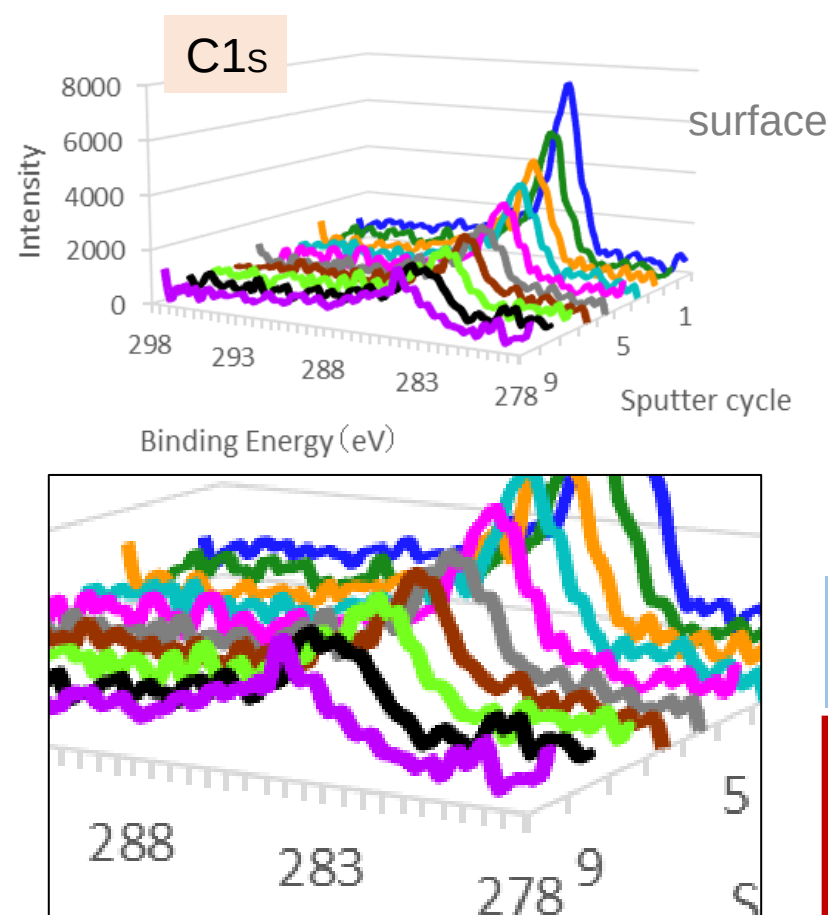
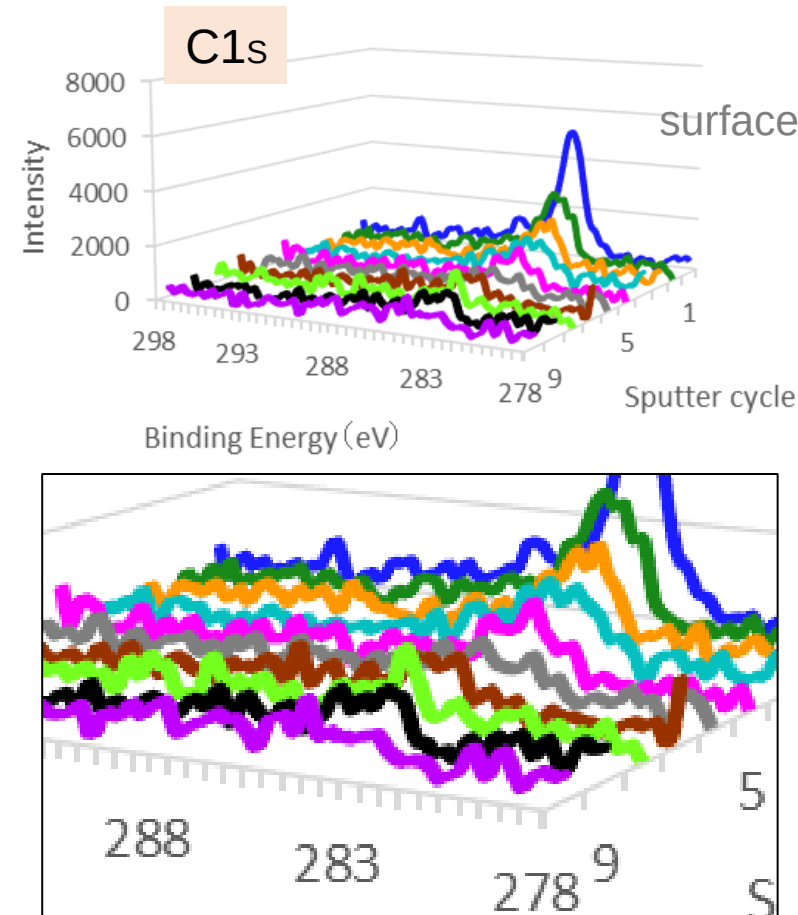
Conventional process

Measurement method
X-ray photoelectron spectroscopy
(Depth analysis)

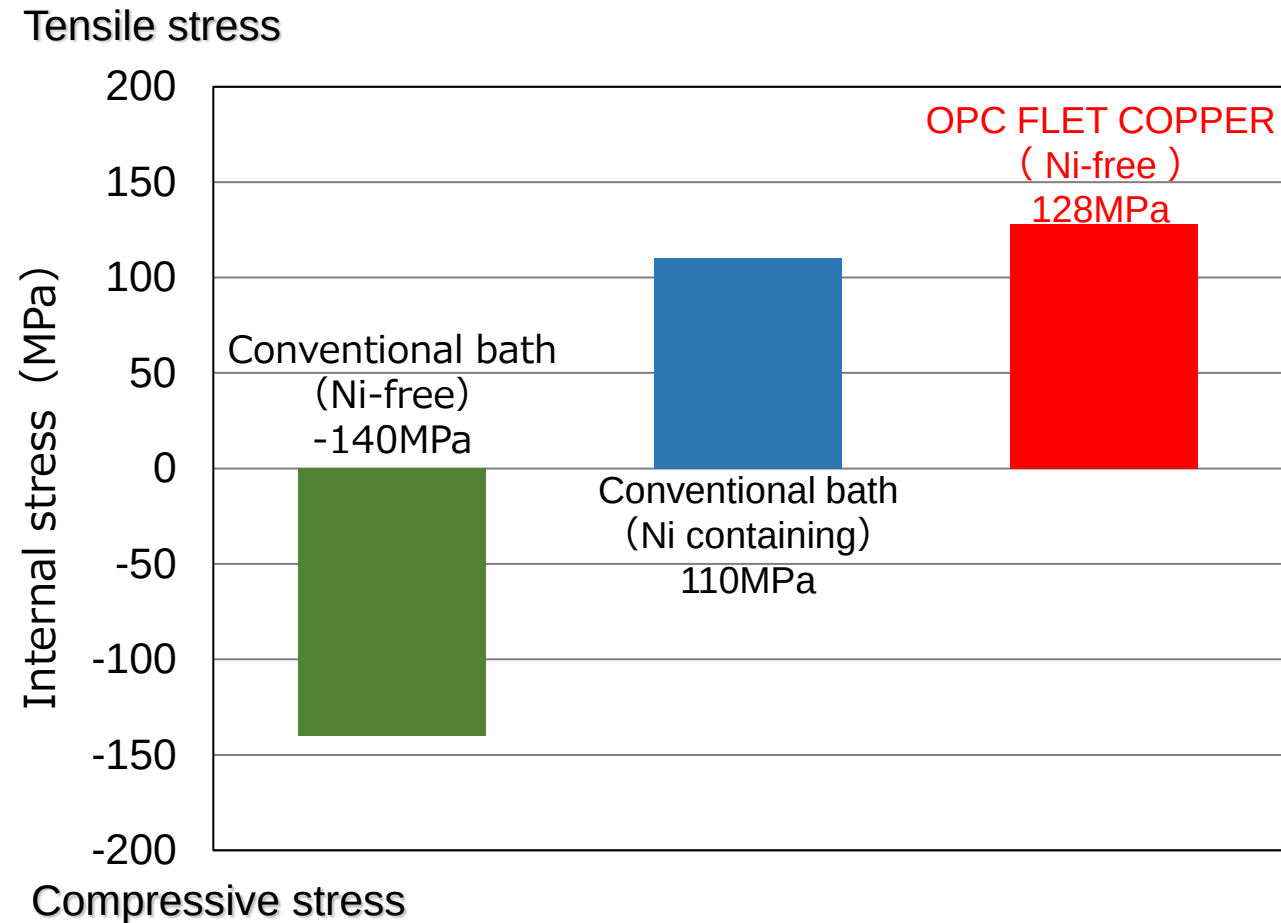


► Compare carbon adsorption amount
by C1s intensity

**Conditioner for OPC FLET PROCESS
can reduce carbon adsorption amount.**



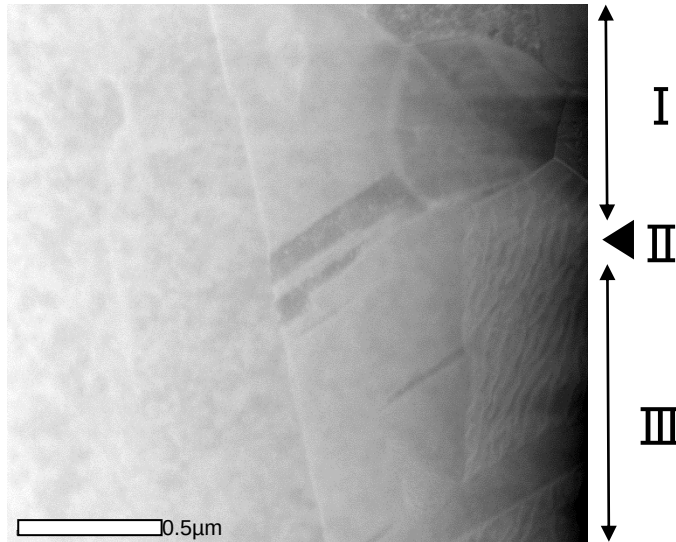
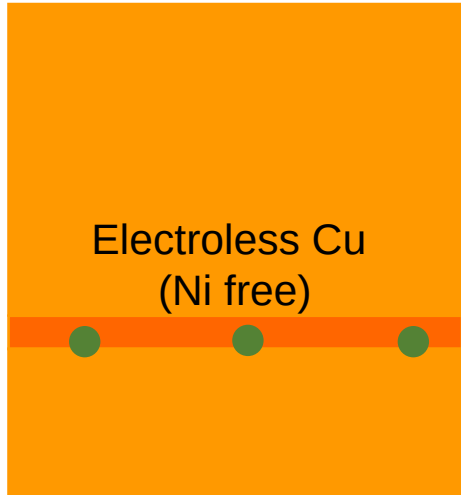
Weak tensile stress without nickel



**Achieve weak tensile stress :128Mpa
By using other stress adjuster (Not Nickel)**

OPC FLET PROCESS

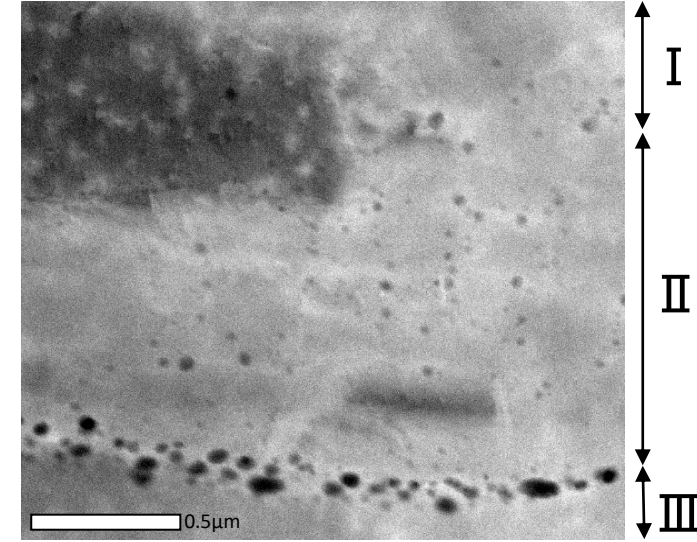
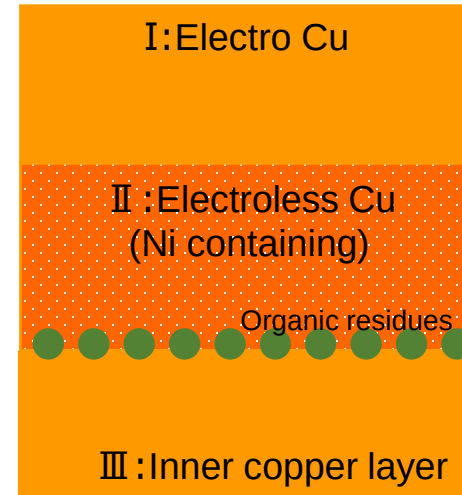
OPC FLET PROCESS



- Organic components: **Less**
 - Electroless copper: **Thin(0.1μm)**
 - Nickel: **Not contained**
 - Hydrogen gas amount in electroless copper plating: **Less**
- Nano Void: less**

STEM image of via

Conventional process



- Organic components: **Many**
 - Electroless copper: **Thick (0.4~1.0μm)**
 - Nickel: **Contained in film**
 - Hydrogen gas amount in electroless copper plating: **Much**
- Nano Void: Many**

STEM image of via

• TEM observation : Flexible 3D system Integration Laboratory at Osaka University

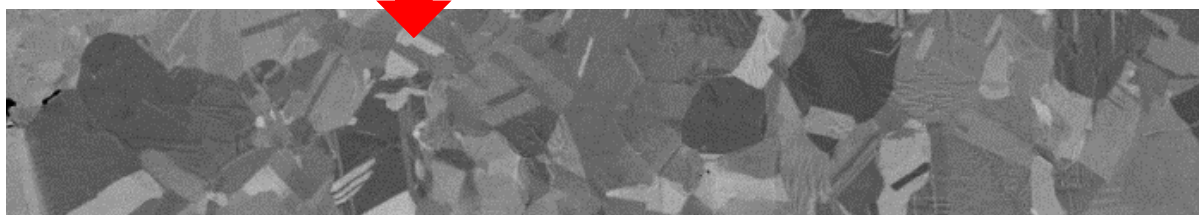
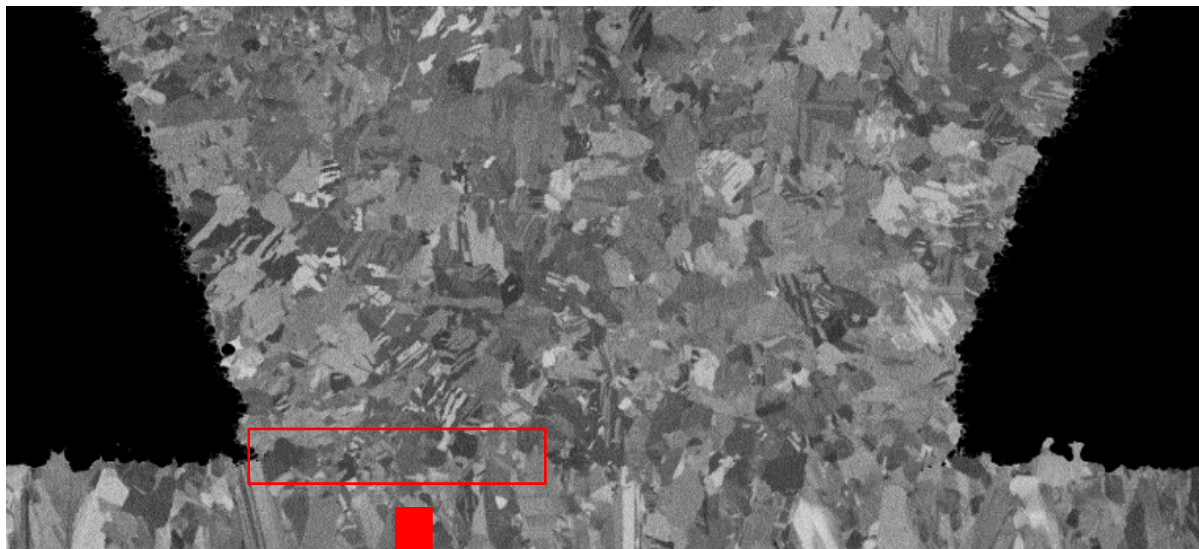
OPC FLET PROCESS: Nano void problem can be solved.

Via-bottom crystal continuity

(Via diameter 80 μm , via depth 40 μm)

Using ABF GL102

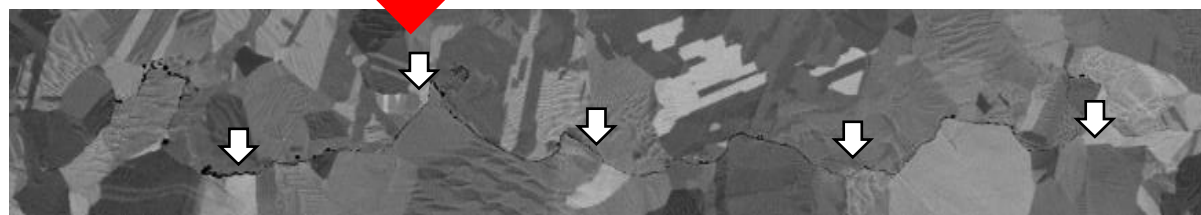
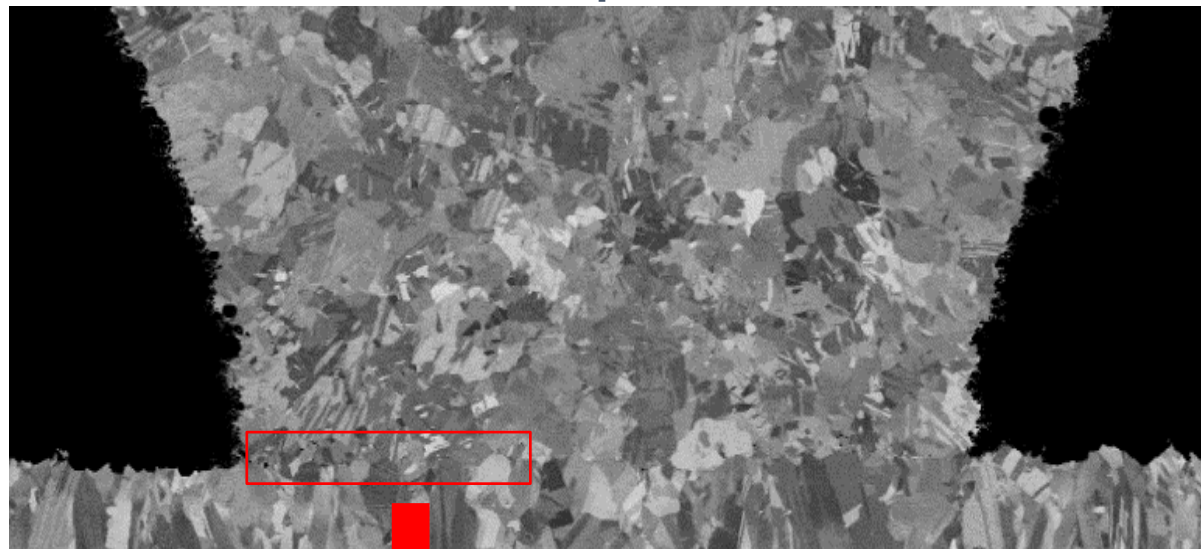
OPC FLET PROCESS



EBSD analysis image



Conventional process



OPC FLET PROCESS: Nano void less and via-bottom crystal continuity can be observed.

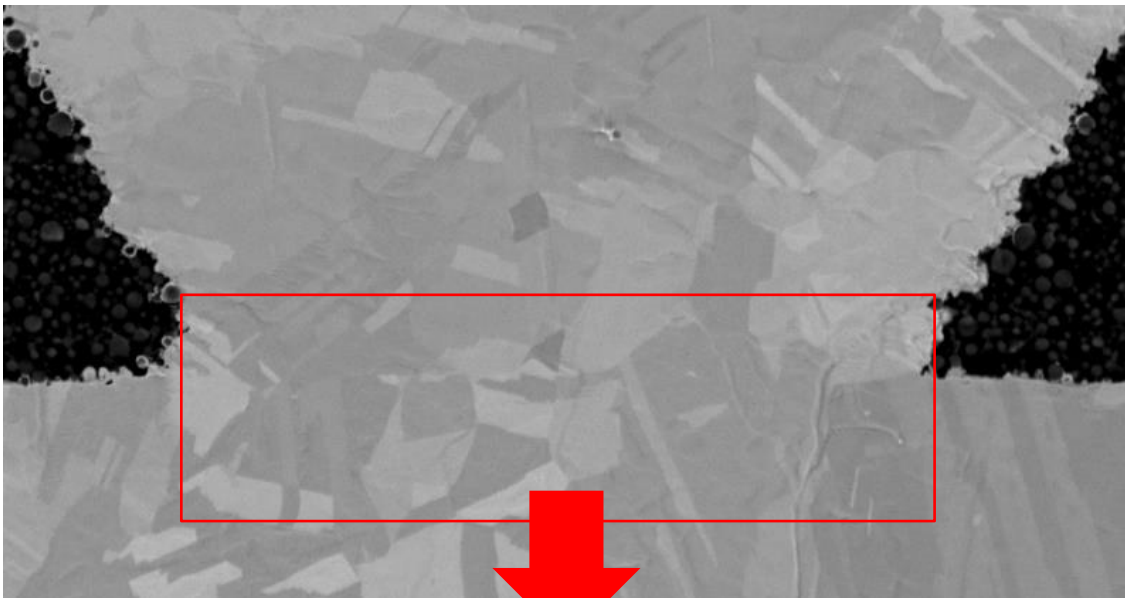
Via-bottom crystal continuity

(Via diameter 15 μm , via depth 15 μm)

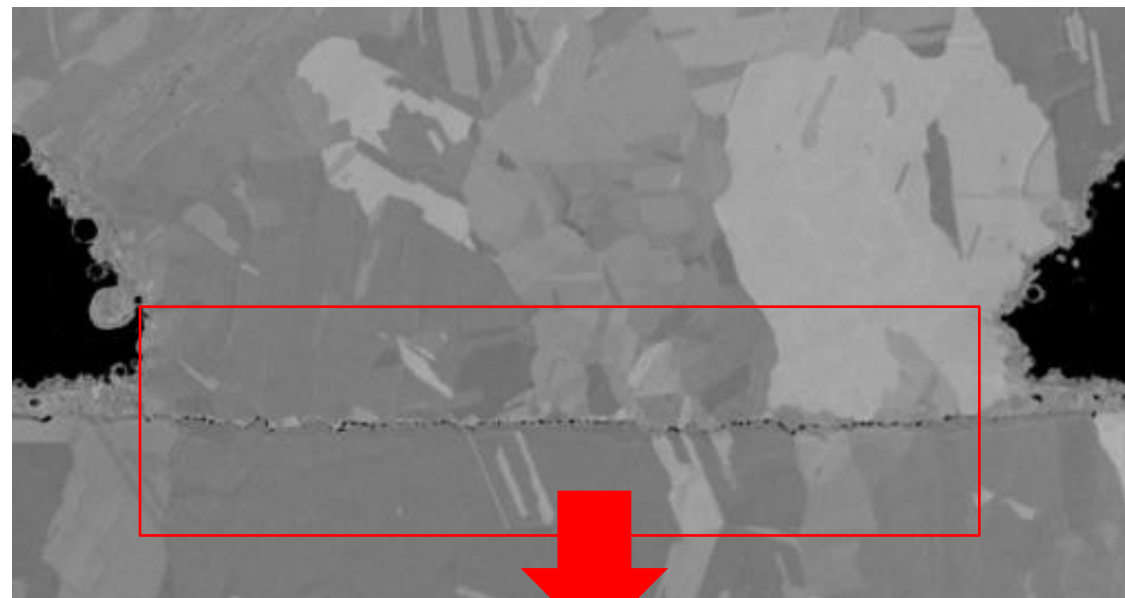
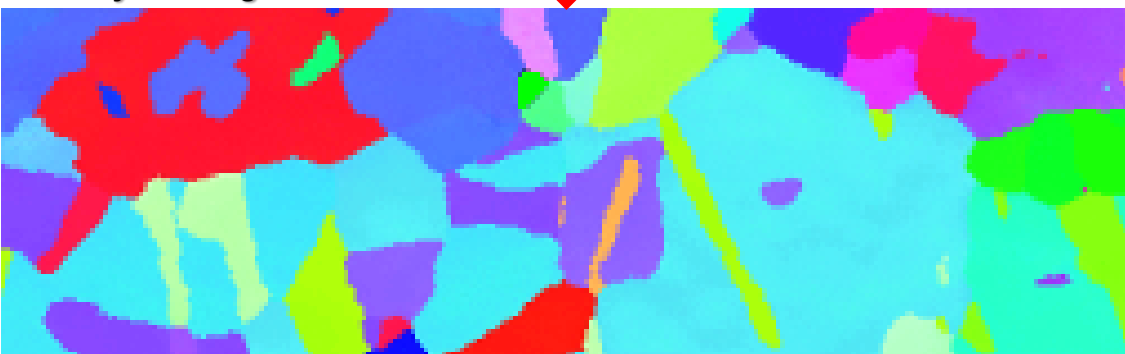
Using ABF GL

OPC FLET PROCESS

Conventional process

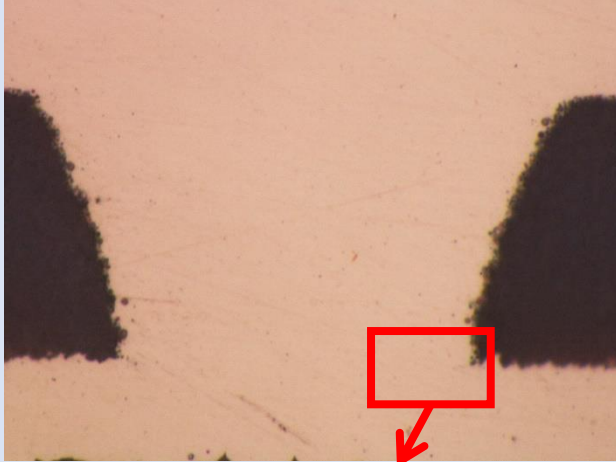
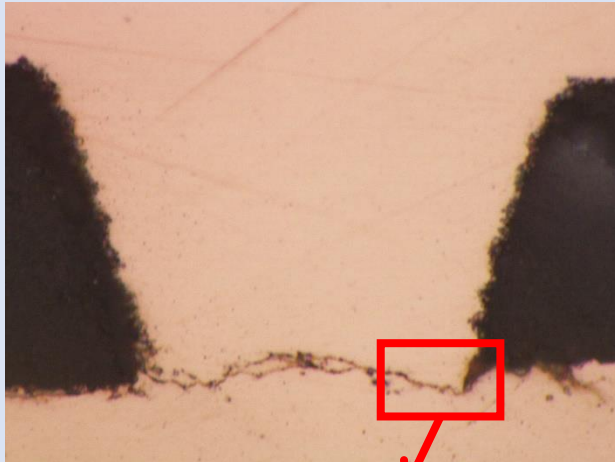
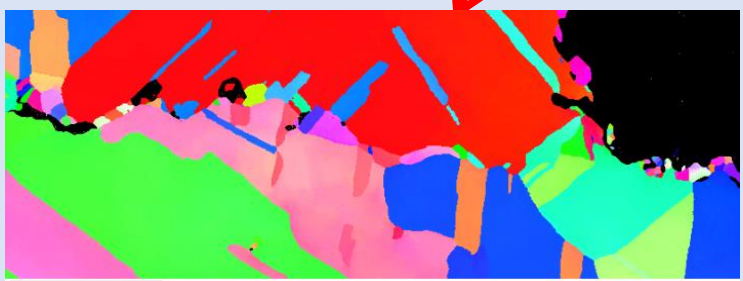


EBSD analysis image



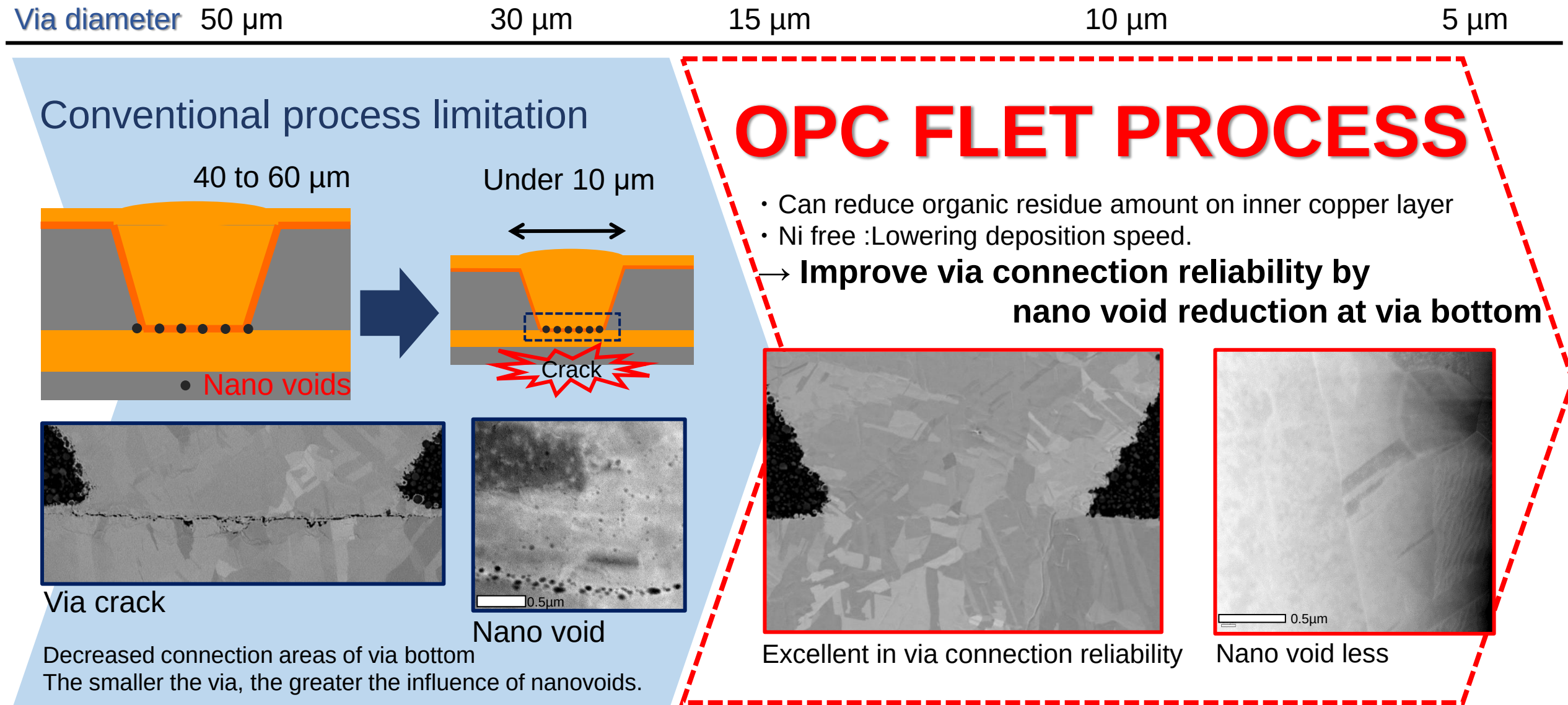
OPC FLET PROCESS: Nano void less and via-bottom crystal continuity can be observed.

Solder heat resistance test

	OPC FLET PROCESS		Conventional process
Solder heat resistance test (Separation/Observed holes)	0/100	NG mode: 0	16/100
Cross-sectional view (Stereomicroscope)			
EBSD analysis image After solder heat resistance test			

- Dipped into 293°C of a tin-copper based solder (ECO SOLDER M20, 99.25Sn-0.75Cu alloy composition by weight, SENJU METAL INDUSTRY CO., LTD.), 10 second dipping time, 10 cycles
- Substrate: ABF GL102, via hole diameter 80 µm, insulation film thickness 40 µm

Summary of OPC FLET PROCESS



For more information, please contact our website.

- Okuno Chemical Industries Co., Ltd. Website <https://www.okuno.co.jp/en/>

- In the website:

ELECTROLESS COPPER PLATING PROCESS FOR IC SUBSTRATES

<https://www.okuno.co.jp/en/product/mf/semiconductor.html>

OKUNO's process for the manufacture of semiconductor package substrates

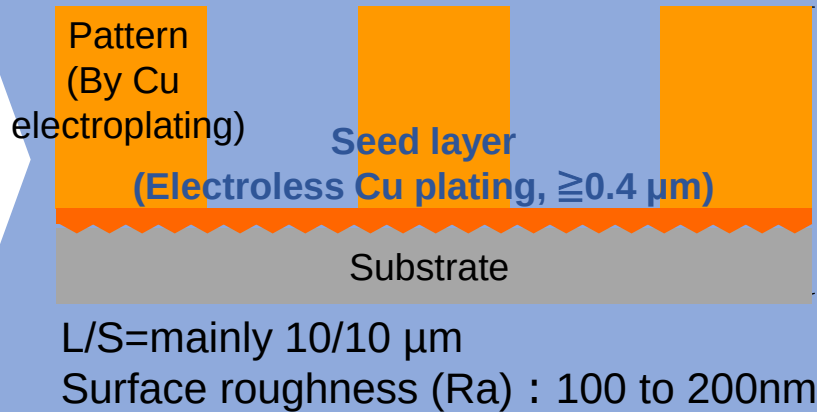
https://www.okuno.co.jp/en/product/process/process_for_ic_substrate.html

Contribute PWB fabrication by OKUNO's total solution

https://www.okuno.co.jp/en/product/process/multi_layer_pwb_process.html

Problem in ultra-micro Cu pattern formation

Now



Next generation

Downsizing

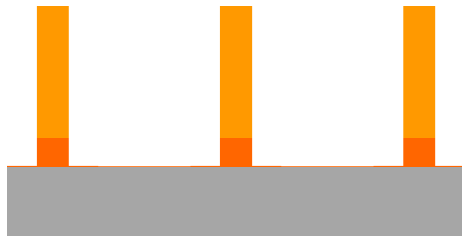


- ① Ultra-fine pattern formation
Under L/S = 5/5 μm
- ② Low roughness substrate
Surface roughness (Ra): under 50 nm

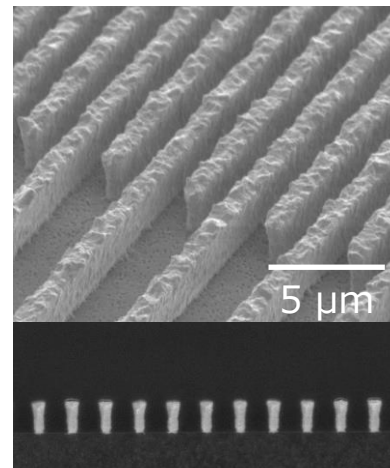
Difficulty in pattern formation

For ultra-micro pattern

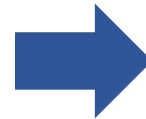
L/S = 1/1 μm



✓ Pattern damage in seed layer etching step



Requirement



- High adhesion to low roughness substrates
- Reduce electroless Cu plating thickness

If electroless Cu thickness reduces in conventional process?

With conventional bath

By lower bath temperature, or by plating time reduction

Increase sheet resistance

Low covering power

Conventional electroless Cu plating bath:
Can't use for reduced thickness

Keyword: nickel-free bath

Control plating speed

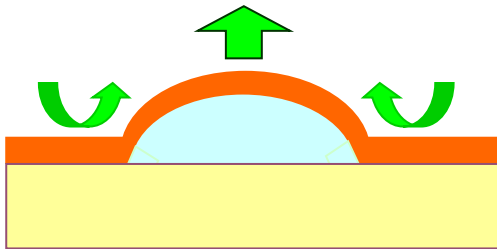
Use other stress adjuster

Conventional electroless Cu plating bath

Conventional bath Film Stress adjustment method

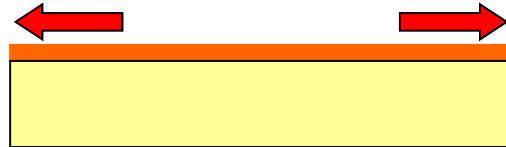
Compressive stress

The film to expand and spread, which leads to blister.



Tensile stress

The tensile stress acts as a pull on the outside.



Nickel is co-deposited on the electroless Cu plating film to adjust to weak tensile stress.

Effect of nickel

	Conventional bath (Ni containing)	Ni free bath
Ni in electroless Cu (% by weight)	1.5	0
Film stress (1.0μm)	110MPa (Tensile)	-140MPa (Compressive)
Deposition on build-up film		
	No blister	With blister
Sheet resistance (Electroless Cu : 0.20μm)	0.67 Ω/□	0.19 Ω/□

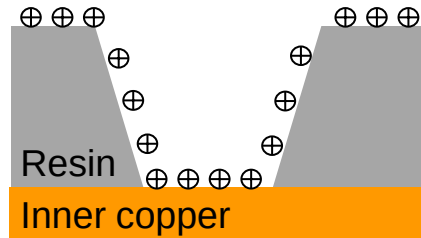
**Weak tensile stress solves blisters,
But reduced film purity, sheet resistance increases.**

Conventional bath :Seed layer thickness 0.4~1.0μm

Electroless copper plating process

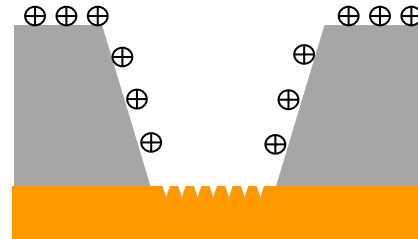
Alkaline ion catalyzing process

Conditioning

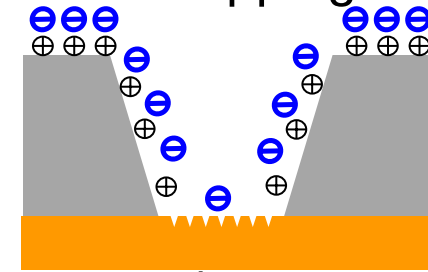


⊕ : Cation component

Soft etching, desmutting

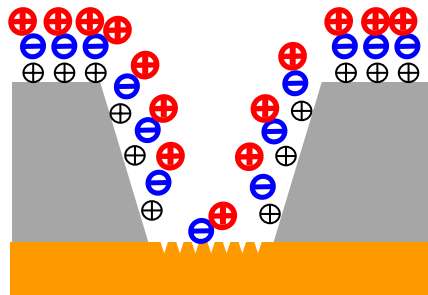


Pre-dipping



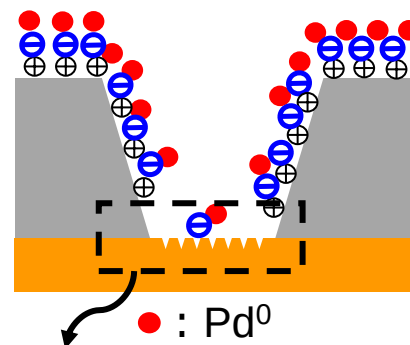
⊖ : Anion component

Pd ion catalyzing



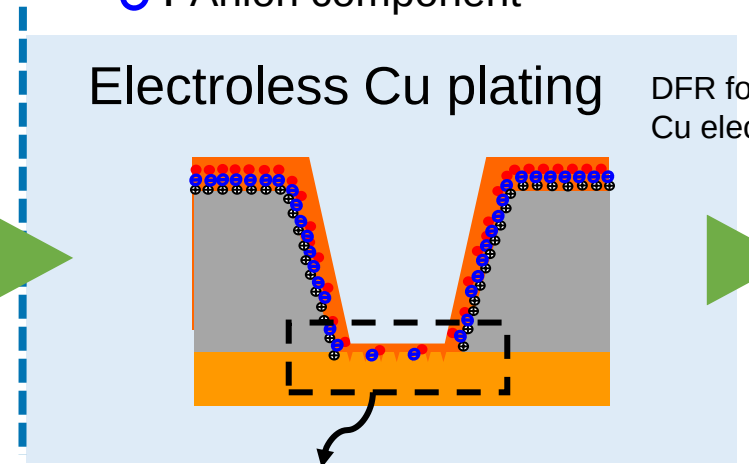
⊕ : Pd ion complex

Activating



● : Pd⁰

Electroless Cu plating



DFR formation
Cu electroplating

Continuous crystal formation and void existence are deeply related to **organic residue¹⁾** on inner copper layer and **electroless copper thickness^{2,3)}** and **purity⁴⁾**

(1) kuribayashi, Y. (2020). To obtain connection reliability at the bottom of via Requirements for Electroless Copper Plating Processes. The Japan Institute of Electronics Packaging, pp. 429-431.

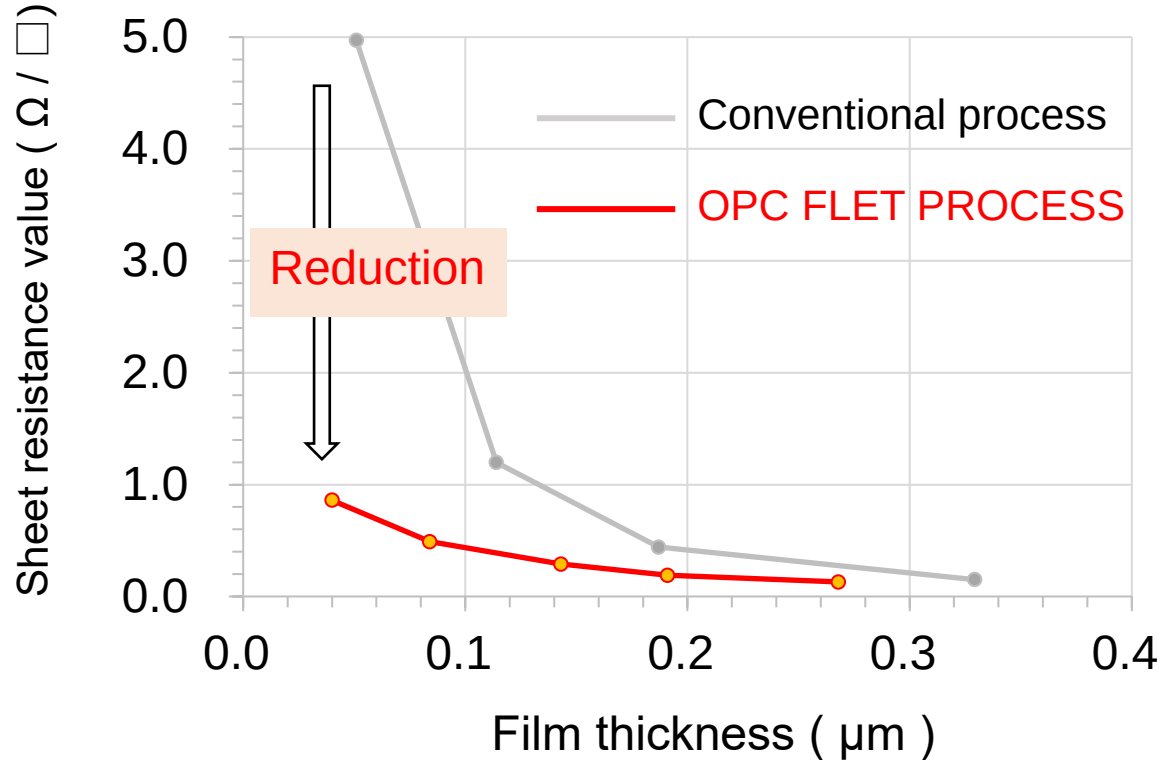
(2) Nakahara, S. (2012). Incorporation of impurities in deposited films. Journal of the Surface Finishing Society of Japan, vol. 63, no. 4, pp. 200-208.

(3) Kondo, K. (2009) Crystal growth and morphology of electrodeposits. Journal of the Surface Finishing Society of Japan, vol. 60, no. 12, pp. 754-760.

4) Honma, H. Kitahara, Y. Kang, J. (2020). J. of smart processing, vol.9, no.5, pp210-215.

Sheet resistance & film stress in reduced thickness

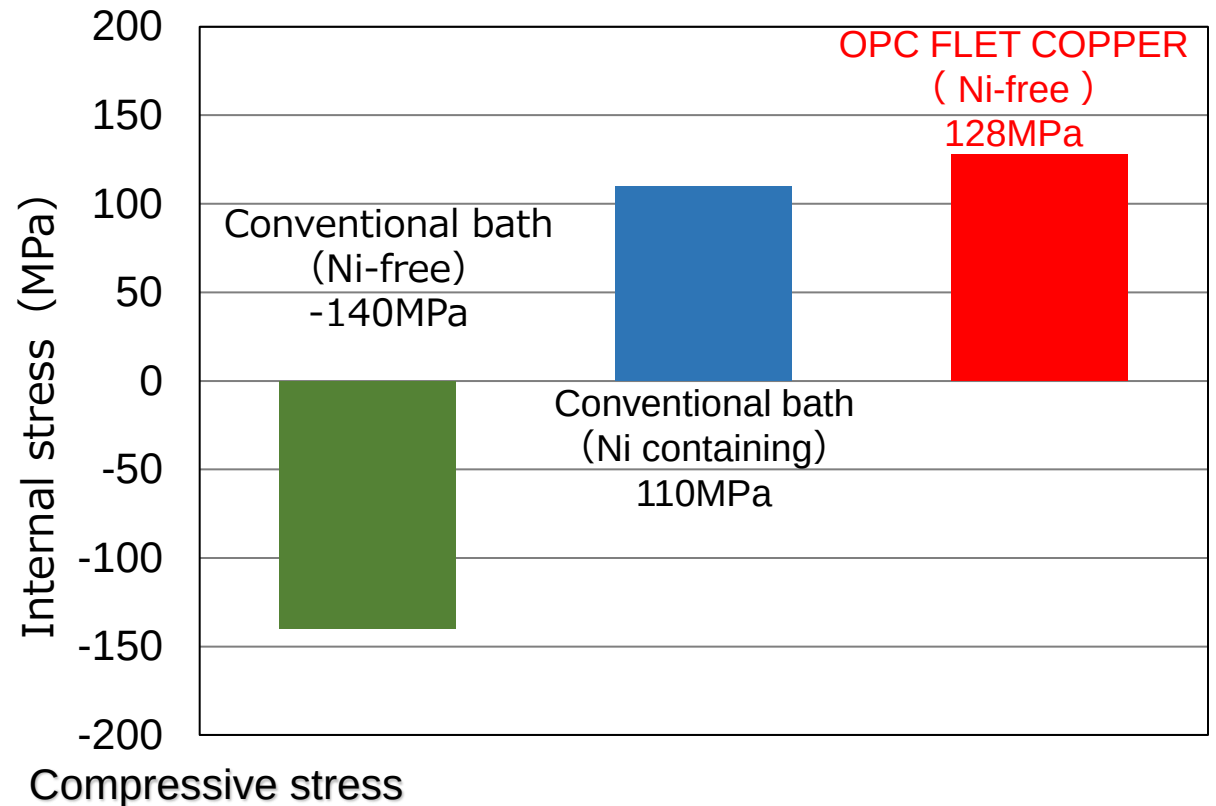
Lower sheet resistance



Ni-free, high copper purity can lower the resistance by small thickness.

Weak tensile stress

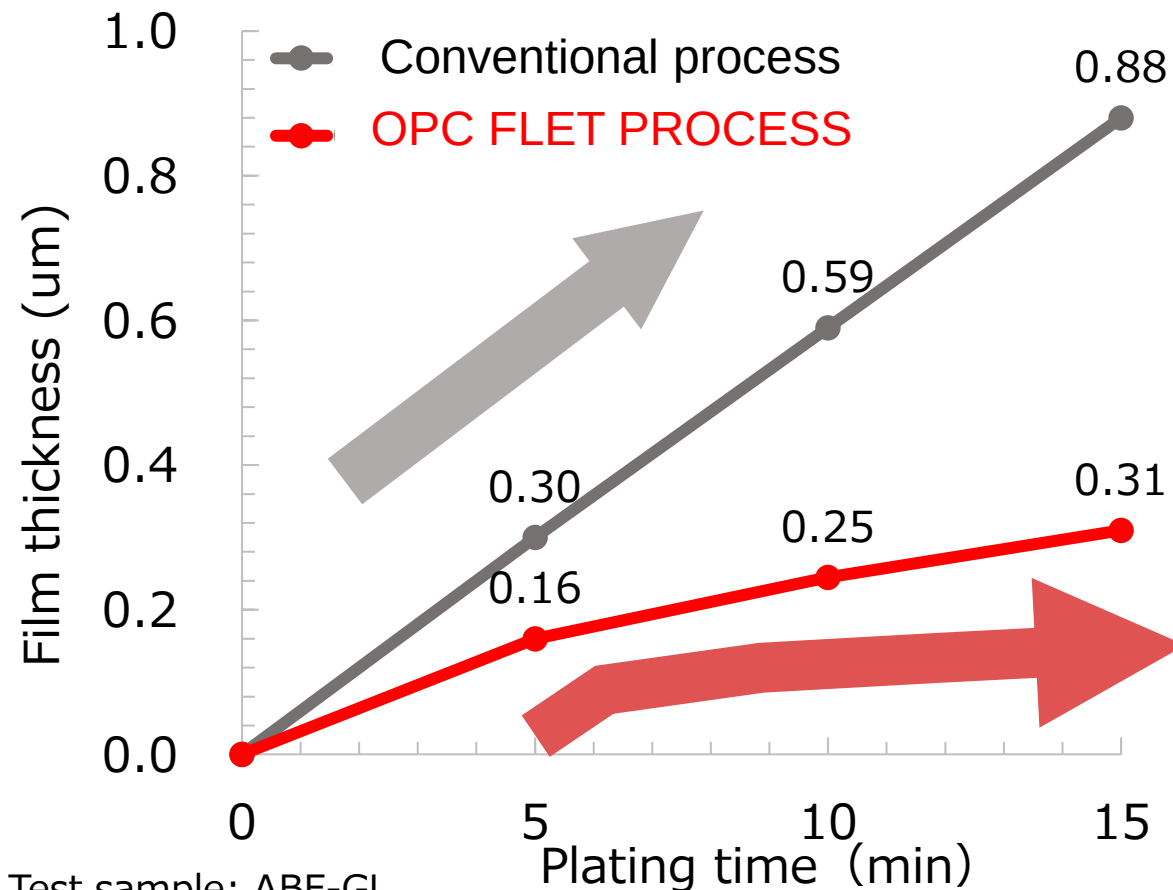
Tensile stress



**Achieve weak tensile stress :128Mpa
By using other stress adjuster (Not Nickel)**

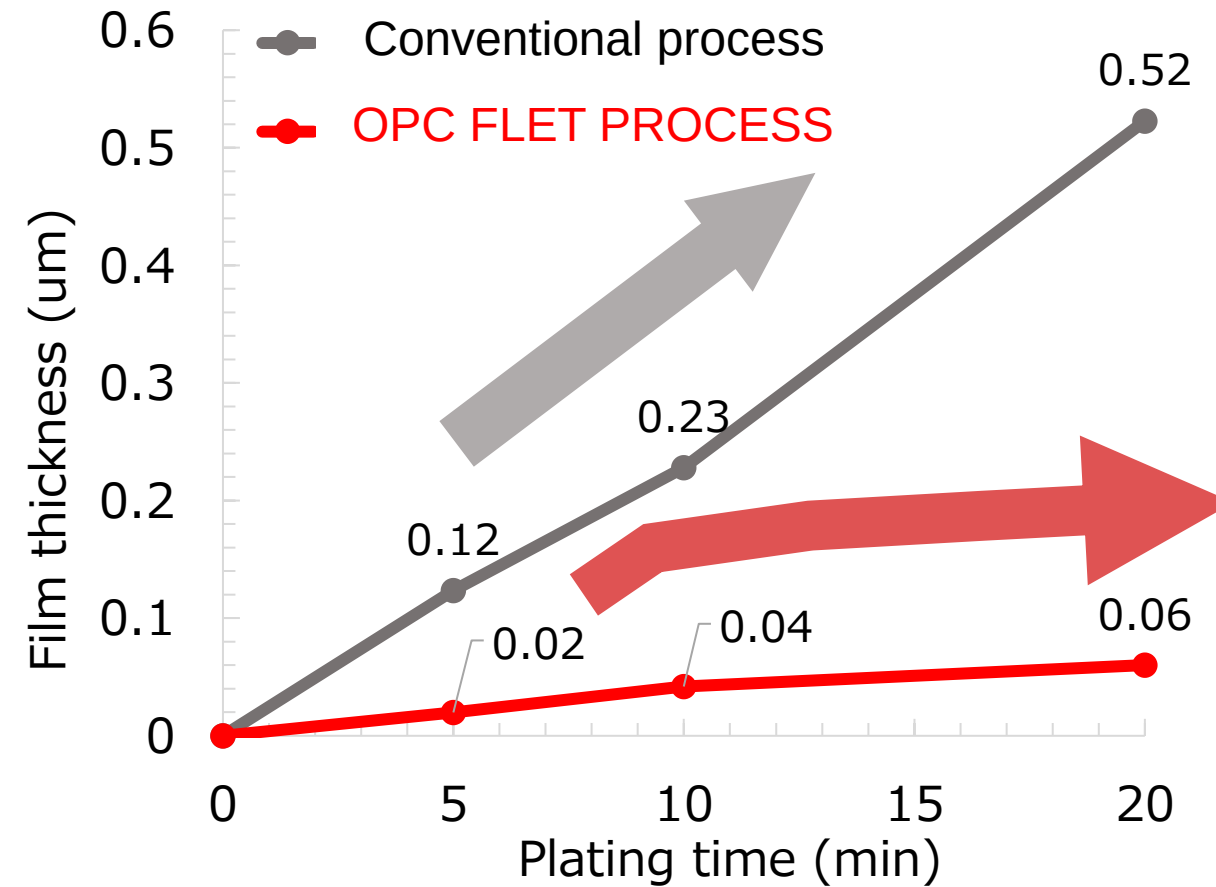
OPC FLET PROCESS : Deposition Rate

ABF resin



Test sample: ABF-GL
(Insulation Build-up Materials; Ajinomoto Build-up Film)

On copper



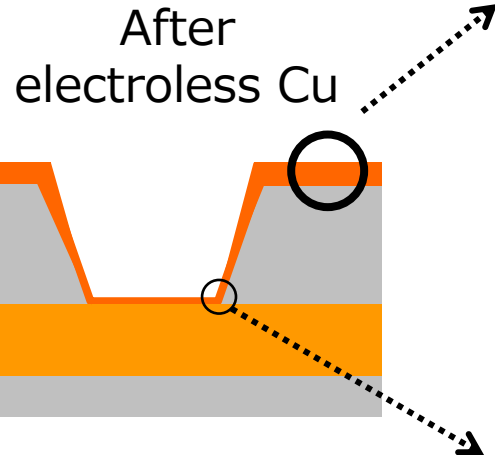
Test sample: Rolled copper sheet

Measured by gravimetric method

Low deposition rate, especially on copper

Via covering power comparison by thinning electroless Cu

Conventional



Problem
Low covering power

Plating film growth			
Surface			
Via bottom			
Initial Plating proceeds			
Throwing power (%)	—	17	20
Large thickness difference			

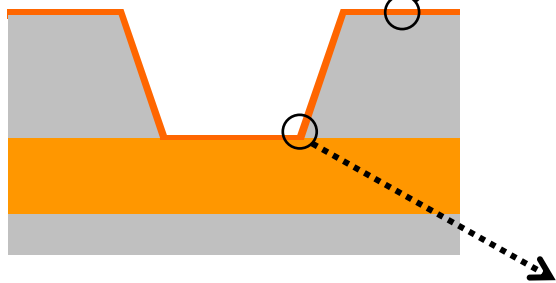
Backscattered electron images of the field emission scanning electron microscope (JSM-7900F, JEOL Ltd.), $\times 50000$

If surface thickness is reduced, sufficient covering power can't be obtained at via bottom.

Via covering power comparison by thinning electroless Cu

OPC FLET PROCESS

After
electroless Cu



Covering power is
controlled

Plating film growth			
Surface			
Bottom			
Throwing power (%)	—	80	100% Small thickness difference

Initial **Plating proceeds** →

Even if surface thickness is reduced, sufficient covering power can be obtained at via bottom.

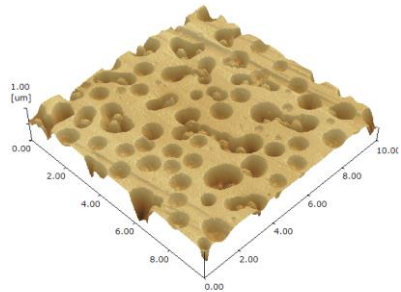
Adhesion test : Peel strength comparison

Toward low roughness insulation films

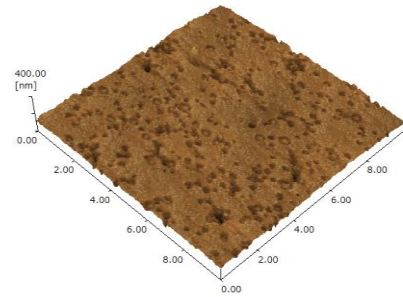
ABF GX-T31

Next generation
ABF GL102

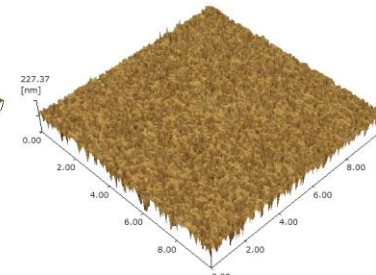
ABF GY50



Ra : 129nm



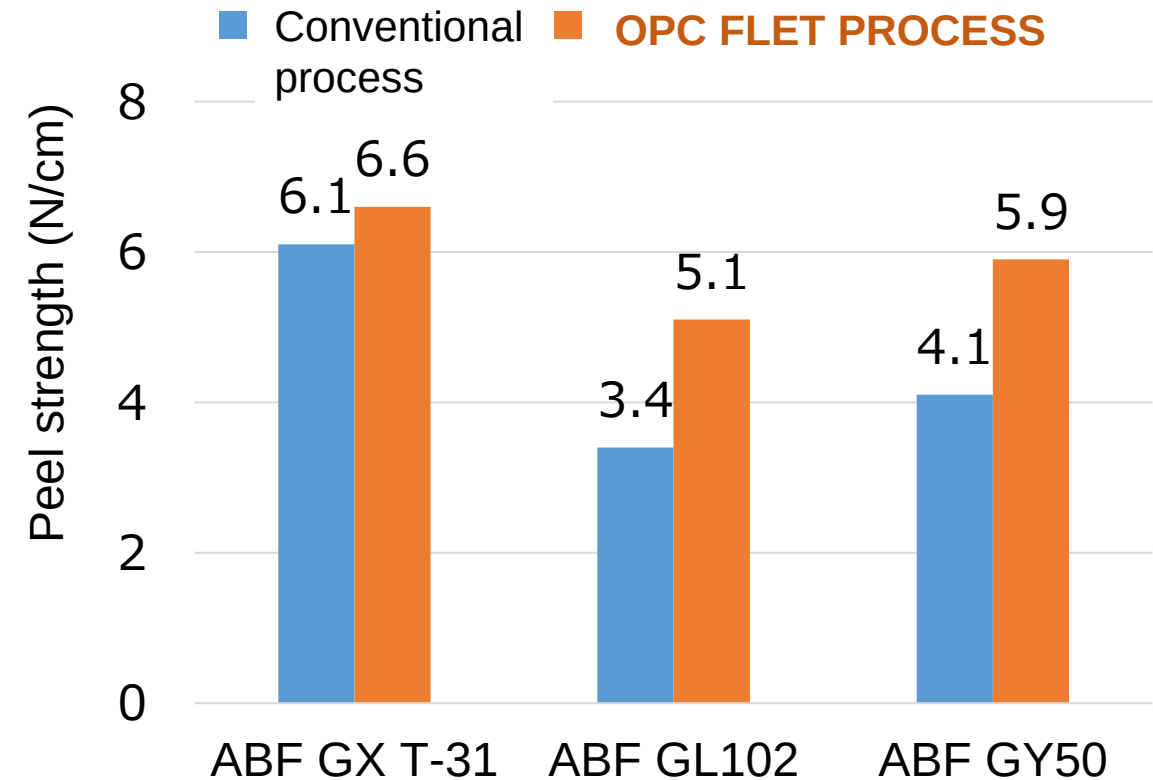
Ra : 10.6nm



Ra : 21.9nm

* AFM surface image
(After desmear)

Peel strength comparison on low roughness material

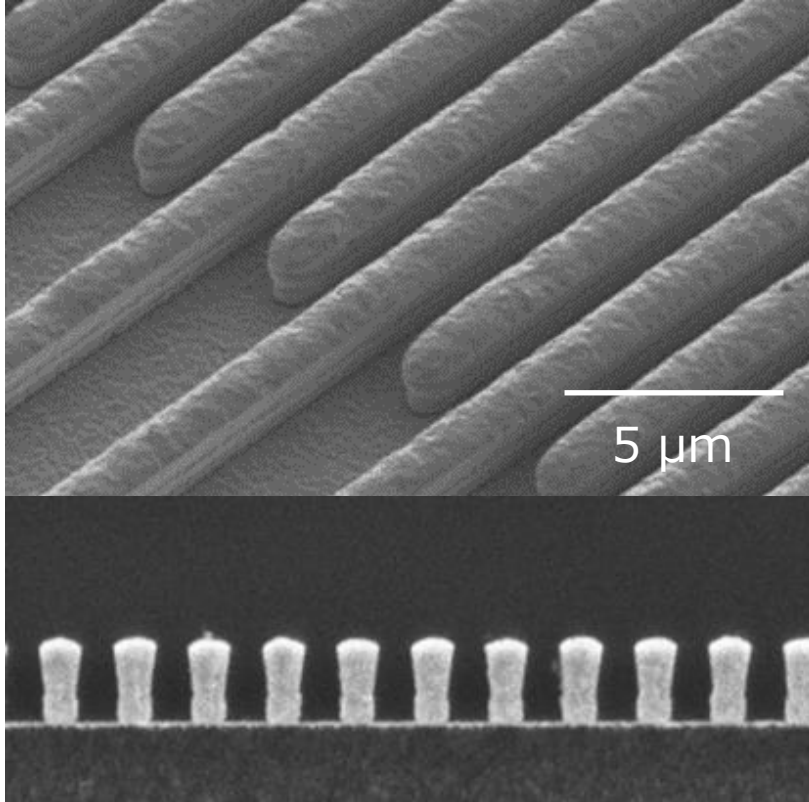


Filler size becomes much smaller
Extremely low roughness

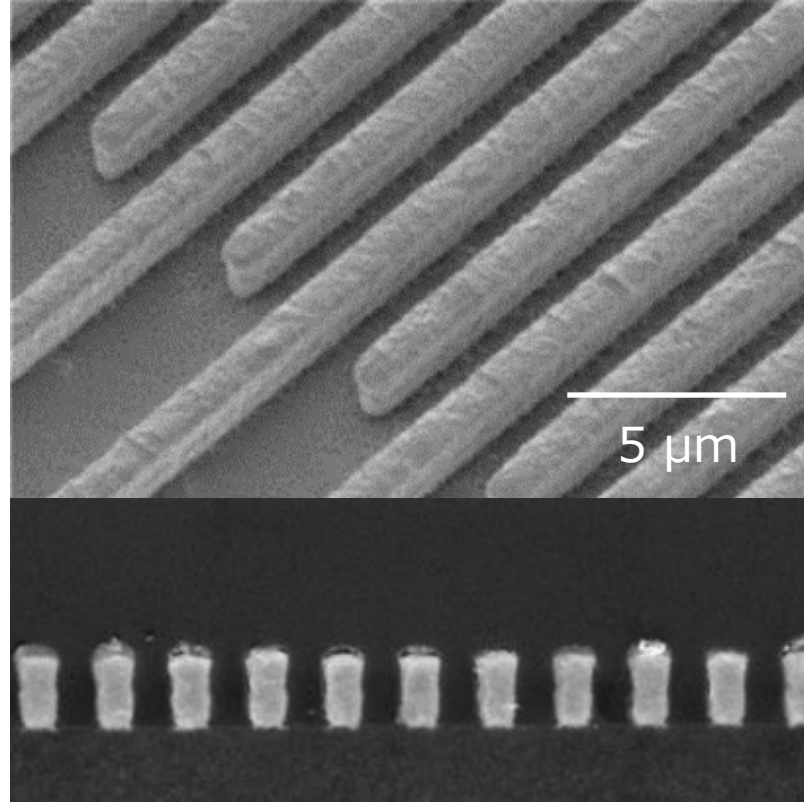
OPC FLET PROCESS indicates high adhesion to low roughness substrates.

Ultra-micro pattern formation for L/S=1/1μm by SAP

Before seed etching

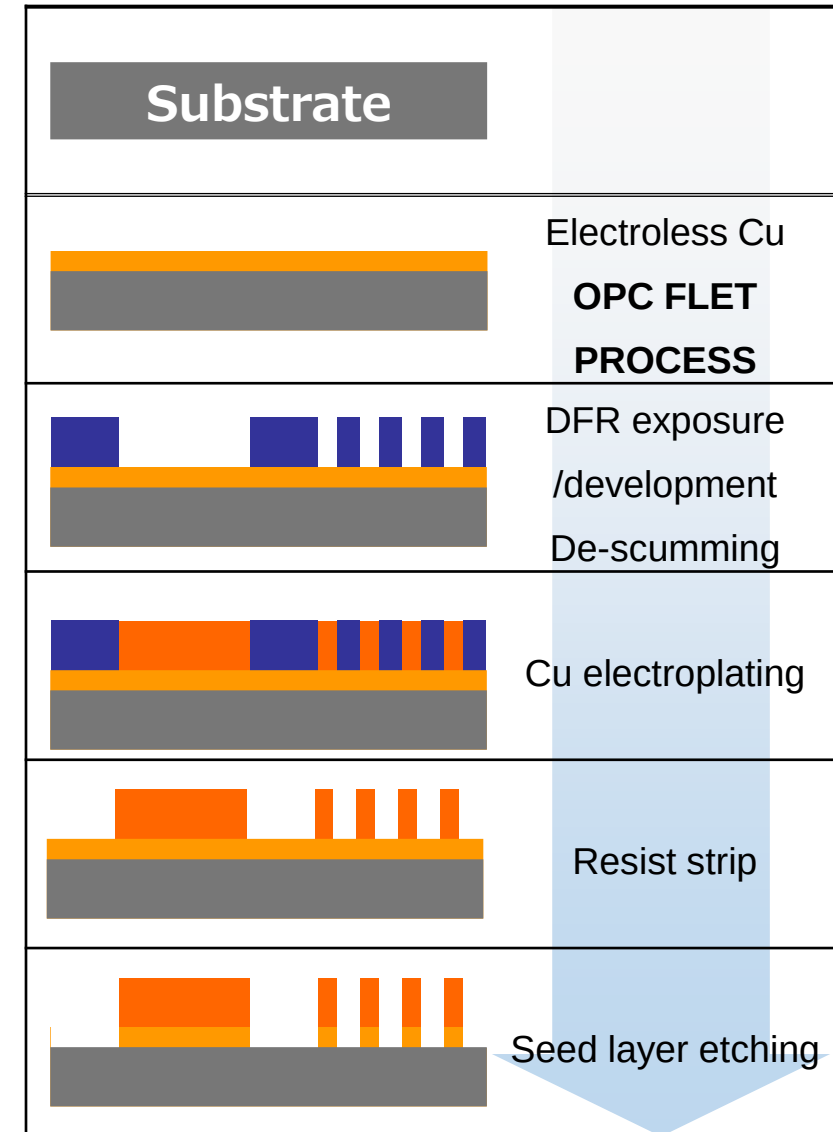


After seed etching



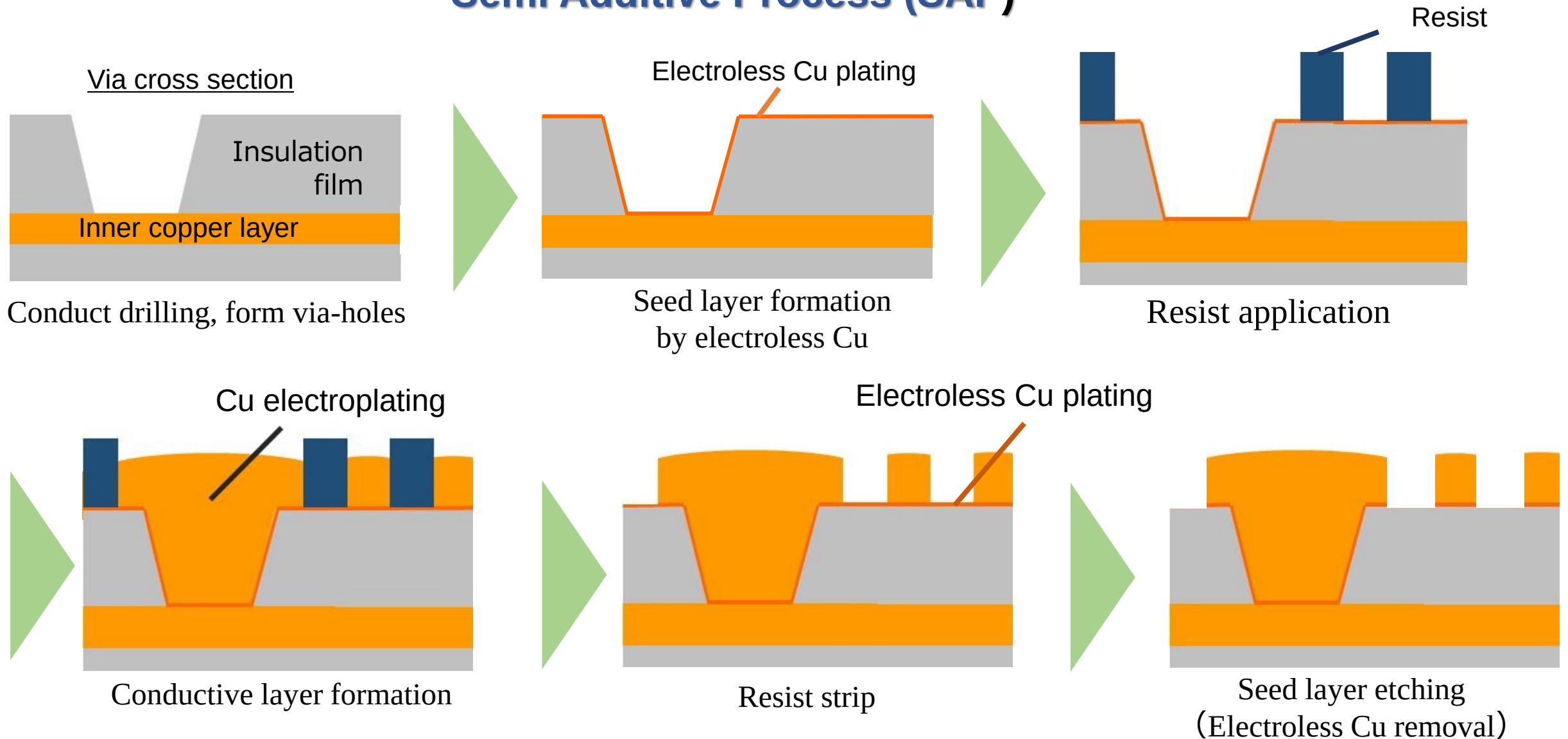
Seed etching amount reduces by thinning electroless Cu.

Protect original pattern shapes, no undercut



Copper pattern formation for IC substrate PCBs

Semi Additive Process (SAP)



Decreased etching amount

Conditioning

Soft
etching

Pre-dipping

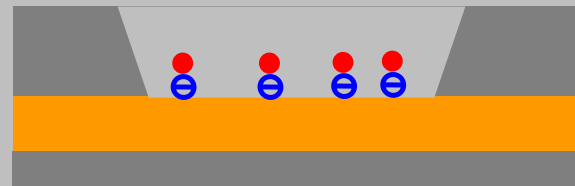
Catalyzing

Accelerating

Electroless Cu
plating

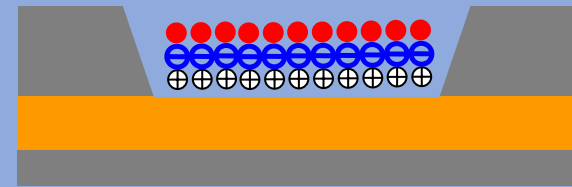
Soft etching amount: conventional

Alkaline ion
catalyzing



Organic residue

Soft etching amount: decreased



- Organic components easily remain
- Catalyst adsorption increase
- Insufficient anchor effect

If organic residue amount increases on inner copper layers,
via connection reliability will decrease.